MAT JOURNALS

Journal of VLSI Design and Signal Processing
Volume 3 Issue 2

A Modified Test Pattern Generation Architecture for Fault Detection in BIST

Ms.M.Nandini Priya
Assistant Professor,Department of ECE,Bannari Amman Institute of Technology, Sathyamangalam, India
nandinipriya@bitsathy.ac.in

Ms.U.Priya
Assistant Professor, Department of ECE, Bannari Amman Institute of Technology, Sathyamangalam, India
priya@bitsathy.ac.in

Ms.D.Preethi
Assistant Professor, Department of ECE, Bannari Amman Institute of Technology, Sathyamangalam, India
preethi@bitsathy.ac.in

Abstract
Multiple test patterns varying in a single bit position is generated for built-in-self-test (BIST). The test patterns generated using Johnson Counter and Seed Vector lacks in fault coverage. So Seed vector block is eliminated and patterns varying in single bit position is generated using 8 bit Johnson Counter has been proposed to have the required fault coverage with reduced test length. The generated test patterns have an advantage of minimum transition sequence. The methodology for producing the test vectors for BIST is coded using VHDL and simulations were performed with ModelSim 10.0b. The Area utilization and the power report were manipulated with the help of Xilinx ISE 9.1 software. The area reduction of 58% and power reduction of 9% is achieved while generating test patterns using Johnson counter.

Keywords: *Built-in-self-test (BIST), Multiple Single Input Change Vector (MSIC), Test Pattern Generator (TPG).*

INTRODUCTION

Testing a circuit every time before they startup, is called Built in Self Test (BIST). The architecture has both test pattern generator and response analyzer on the circuit that is to be tested. BIST reduces using costlier ATE and the time needed for testing. The block diagram of BIST contains test pattern generator, circuit under test, response analyzer and test controller. The signal start test is given to test controller, the test patterns are generated using test pattern generator. The generated patterns were applied on circuit that is under test. The response analyzer block compares the response of the circuit with the predicted response. If the response of the circuit matches with the predicted response the pass signal is provided to the test controller else fail signal is provided. Based on pass or fail signal obtained by the test controller, the signal accept or reject is provided to the user. The patterns can be generated using ROM, LFSR, counter. The CUT may be combinational or sequential circuit. The response analyzer can be comparator or an LFSR utilized as signature analyzer.

Test patterns required for testing is determined using Automatic Test Pattern Generator (ATPG) which is to be applied as input to the circuit. The vectors produced were utilized by the circuit to

identify the faults in manufacturing and to determine the cause of failure. The patterns can be generated using three techniques namely Exhaustive, Pseudo exhaustive and Pseudo random testing. ATPG process involves in fault activation and fault propagation. The value of the signal becomes opposite during the process of activating the fault. The activated fault is moved forward by path sensitizing to the output known as fault propagation. The effectiveness of ATPG is measured by the ratio of faults identified to number of test vectors required.

The patterns generated using BIST are multiple single input change vector which vary in single bit position. The power dissipation is caused due to static and dynamic power dissipation. Static power is consumed only when the device does not operate. Hence occurrence of power dissipation is due to dynamic power dissipation. The main cause for dynamic power dissipation is because of continuous switching of bits.

The power dissipation is given by the equation $P=C_L V^2 F$, where V represents the supply voltage, CL is the value of capacitance at gate output, F is the switching frequency. The parameters influencing dynamic power dissipation are supply voltage, switching activity and clock frequency. The reason for large dissipation of power is due to change of state. Since nodes in digital circuit have to and fro transition between two logic levels, the capacitor at the output charges and discharges continuously. Fraction of the energy is stored at the capacitor and the remaining energy gets dissipated as heat. The circuit is subjected to irreversible damage because of extreme heat dissipation during charging and discharging process. Undesirable switching is reduced by generating patterns with increased correlation among subsequent test vector. This increased temperature caused by unwanted toggling affects the reliability of the circuit. To overcome these draw backs the patterns were generated with reduced toggling activity.

BIST approach is used for internal testing in digital system. The constraints restricting the parallel operation occurring at BIST are area, power and delay. Testing becomes complicated process as the devices are packed in multi-chip modules. To overcome these difficulties in testing multilevel BIST strategy were used in [1]. BIST scheduling process is provided which helps in power reduction by testing the blocks individually. Rather testing the device as a whole, the blocks distributed on various stages were tested individually.

P.Girard in [2] performed a survey on various external and internal testing methodologies. The power consumption of the device during the process of testing is higher when compared with the normal operation.

In order to curtail subsequent test transition, bit swapping LFSR (BS-LFSR) technique is adopted in [3]. Parallel testing operation is performed to reduce the test time. Girard et al. analyzed the energy reduction without using additional area and delay overhead [4]. The analysis is performed to select the appropriate seed vector for LFSR for the purpose of energy minimization. The heuristic method is adopted leading to reduction in the energy consumption.

Wang and Gupta employed two distinct LFSR with varying speed to shrink the changeover of input bits [5]. A test pattern generating technique for minimizing the power requirement in combinational circuits has been proposed in [6]. The test patterns were generated using cellular automata. This method helps in achieving high fault coverage and minimizing the

power requirement. A modified clock scheme for BIST technique [7], was used to reduce the power dissipation. Two different clocks are used for the test pattern generation rather than the single clock. The data path consists of module with larger size and results in increased complexity. So in [8] the deterministic patterns have been produced for the purpose of testing data paths.

In [9] Bonhomme et al introduced the gating of clocks to minimize the power dissipation. The first clock controls the odd scan cell and the next clock pulse controls the even scan cell. In [10] Laoudias.C et.al constructed the ring generator for the purpose of producing test vectors. The results obtained are compared with the forecasted result. S. Bhunia et al. in [11] placed additional transistors at the ground path to obstruct the toggling of bits at the input. Unwanted transition is masked at the input to reduce the activity of switching thereby minimizing overall power. Efficient partial scan cell gating [12] was used to identify the representative lines. During scan based testing the selection and gating is done based on representative lines. P. Girard et al in [13] proposed hybrid solution combining reseeding technique and vector controlling technique to handle the increased power activity during testing.

The rest of the paper is organized as follows. In Section I, the Existing Methodology is presented. In Section II, the Proposed Methodology is presented. In Section III, the Simulation results and analysis is presented. Conclusion is given in Section IV.

EXISTING METHODOLOGY

The Existing technique generates the test pattern using Reconfigurable Johnson counter and the seed vector. Test patterns were generated by performing Exclusive-or operations between Johnson counter and seed vector.

Test Pattern Generation Method

The test pattern generation architecture contains Reconfigurable Johnson counter and seed vector block. Test patterns were generated by performing Exclusive-or operations between Johnson counter and seed vector. The vectors obtained were utilized by the scan chain. The pattern generation method for BIST shown in Fig.1 involves performing Exclusive-or operation between the seed vector and reconfigurable Johnson counter.

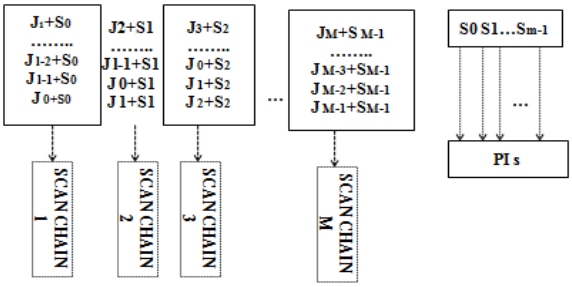

Fig 1. *Symbolic Representation of an MSIC pattern*

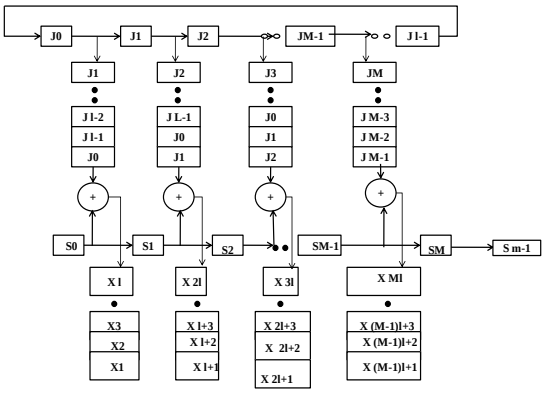

Fig 2. *Applying MSIC vectors to scan chain*

The generated patterns were applied to the scan chains as shown in the Fig.2. The Reconfigurable Johnson counter generates Johnson vector and the seed block generates the seed vector. The results obtained were loaded into the scan chain.

The vectors are circularly shifted continuously and Exclusive-or operation is performed with the seed vector. The procedure is repeated until all the scan cells are loaded. The eight bit patterns generated were tested on 4*4 Multiplier circuits.

MSIC Test per clock schemes

The Exclusive-or gate receives input from reconfigurable Johnson counter and seed generator. The clock signal CLK1 and CLK2 were generated using clock and control circuit. The clock signal CLK1 is applied to seed generator block to produce seed vector. The clock signal CLK2 is applied to Johnson counter block to produce Johnson vector.

The following procedure is adopted to generate the patterns

1. The clock signal CLK1 is clocked to produce the seed.
2. The clock signal CLK2 is clocked to produce Johnson vector.
3. Generate 2l Johnson vectors by repeating step 2.
4. Steps 1-3 were repeated until the specified test length is achieved.

I. PROPOSED METHODOLOGY

Challenging areas in VLSI are cost, area and power. The demand for the portable devices is increasing rapidly. Hence Area and Power optimization are necessary. Here the design for generating test patterns for BIST is presented. The generated test patterns are applied to circuit under test. The response obtained is compared with the known result to verify the correctness of the circuit. The test patterns generated were applied on S344 circuit. The exact functioning of the circuit is verified by comparing with the known result as shown in Fig 3. This method is suitable for detecting faults in a combinational circuit.

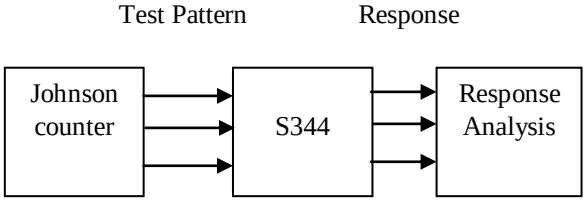

Fig 3. *Testing of VLSI Circuits*

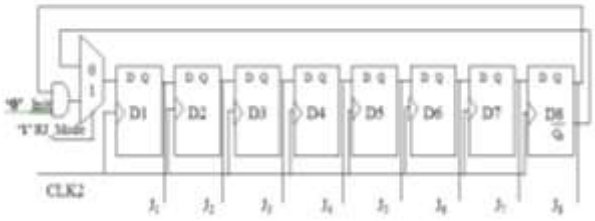

Fig 4. *TPG using Johnson counter*

The idea behind the test pattern generation using Johnson counter is to detect faults with least test length. To cover all possible stuck-at-faults with least test length the architecture is modified by eliminating the accumulator architecture.

Johnson Counter Architecture

The single input change test patterns were produced using Johnson counter. The required fault coverage is attained with least number of patterns. The proposed TPG using Reconfigurable Johnson counter architecture is shown in Fig 4. This architecture is capable of working under three different modes. During First clock cycle, initialization process is performed to bring the flip flops to the known value. During second clock cycle, reconfigurable Johnson counter operates in normal mode. The select input of the multiplexer RJ_Mode is '0'. The output Q8 corresponding to D_8 flip flop is fed back to D_1 flip flop. For the third clock cycle, reconfigurable Johnson counter operates in circular shift register mode. The select input of the multiplexer RJ_Mode is '1' and Init is set to '1'. The output Q8 corresponding to D_8 flip flop is fed back to D_1 flip-flop. The test procedure is repeated until the required patterns are obtained.

Johnson vectors are generated using Reconfigurable Johnson counter. Here Johnson counter is reconfigured to operate in three distinct modes.

Initialization

Reconfigurable Johnson counter is initialized by setting the value of RJ_Mode to 1 and Init to 0. The CLK2 is clocked until the flip flops are initialized to a known value. Fig. 5 shows the initialization operation of the Reconfigurable Johnson counter.

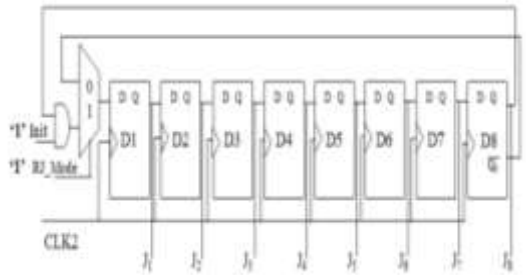

Fig 5. *Initialization mode*

Circular shift register mode

The circular shift operation can be performed by assigning the values of Init and RJ_mode to 1. Fig 6 shows the circular shift operation of Johnson Counter.

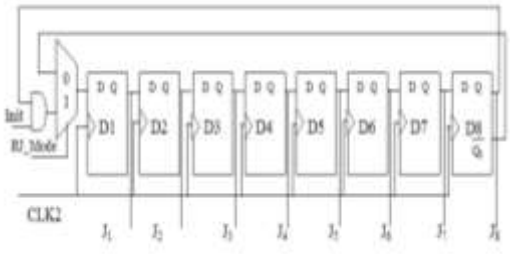

Fig 6.*Circular Shift Register Mode*

Normal mode

The select input of the multiplexer RJ_MODE is assigned to the value 0. The Q8 bar output corresponding to D8 flip flop is feedback. The Normal operation of Reconfigurable Johnson counter is shown in Fig 7.

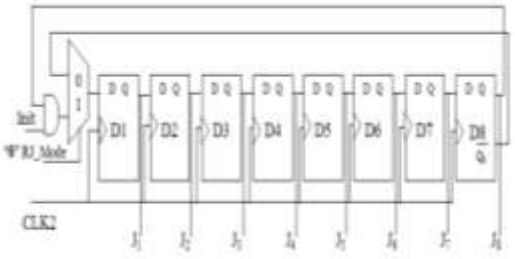

Fig 7. *Normal mode*

The proposed architecture has an advantage of occupying lesser gate count thereby minimizing the complexity of the circuit. The patterns generated vary in single bit position that reduces the unwanted transition thereby reducing the power requirements.

SIMULATION RESULTS AND ANALYSIS

The various design of the test pattern generation for BIST is implemented using front end. The design is coded in VHDL and simulated using ModelSim 10.0b software. The test patterns generated were tested on 4*4 Multiplier circuit. The analysis of area and power are performed using Xilinx ISE 9.1 software.

RECONFIGURABLE JOHNSON COUNTER

The simulation results of test pattern generation using Reconfigurable Johnson counter is shown in the Fig 8. For the First clock pulse the Johnson counter is initialized to a known value by applying mode_sel to ‘00’. The Johnson counter is initialized to ‘11111000’. For the next clock pulse the Johnson counter is operated in normal mode by applying mode_sel to ‘10’. The output of the normal mode pattern_out is ‘11111100’. For the next clock pulse the Johnson counter is operated in circular shift mode by applying mode_sel to ‘01’. The output of the normal mode pattern_out is ‘01111110’. The test pattern generation process is continued until the required fault coverage is attained.

Fig 8. *TPG by employing reconfigurable Johnson counter*

Fig 9. *Testing by employing Johnson counter*

Testing of Multiplier using Reconfigurable Johnson counter

The simulation result for generating the testing multiplier circuit by applying test patterns generated using reconfigurable Johnson counter is shown in the Fig 9. The clocking is provided to generate Johnson vectors. The output signal ref_out is the expected result and test_out is the output after injecting the test patterns. Here fault v is set to the value "000011" indicating s-a-1 fault at second input bit of multiplier. When the vectors of ref_out and test_out are equal, then the pattern is incapable of detecting the fault at that position. Here the pattern "00111111" is applied on the multiplier circuit and the expected result of the multiplier circuit ref_out is "00101101". But the result obtained after injecting s-a-1 fault at second input bit of multiplier circuit test_out is "01101001". The results of ref_out and test_out obtained by applying the vector "11111100" are different. Hence the pattern "00111111" is capable of detecting s-a-1 fault at second input bit of multiplier.

ANALYSIS REPORT

Analysis of area, power, test length and delay for generating test patterns using Reconfigurable Johnson Counter is as shown in Table 1. For implementation 132 gates were required. The total power estimation is 38.08 mW and delay is 6.216ns. The total number of patterns required to cover all possible stuck-at-faults is 7.

TABLE *ANALYSIS REPORT*

Table Head	**Table Column Head**			
	Area (Gate count)	***Power (mW)***	***Test Length***	***Delay***
Existing Methodology	312	41.79	12	11.171
Proposed Methodology	132	38.08	7	6.216

CONCLUSION

The architecture for generating test patterns varying in single bit position for BIST is proposed. The required fault coverage is attained with least number of patterns while generating test patterns using Johnson Counter. Pattern generation using Johnson counter is proposed to have optimized area, power, test length and delay. The single input change patterns generated to improve the correlation between the successive test patterns thereby reducing power requirements. This technique to generate the multiple test patterns varying in single bit position for BIST schemes is coded using VHDL and simulated using ModelSim 10.0b. The gate count and power consumption of the test pattern generation were analyzed using Xilinx ISE 9.1 software. 100% fault

coverage is achieved and time coverage is same as time required for generating patterns using existing methodology. The area reduction of 58% and power reduction of 9% are achieved while generating test patterns using Johnson Counter counter.

REFERENCES

1. Y. Zorian, 'A distributed BIST control scheme for complex VLSI devices,' in 11th Annual IEEE VLSI Test Symposium, April 1993, pages 4–9.
2. P. Girard, 'Survey of low-power testing of VLSI circuits,' IEEE Design & Test of Computer, volume 19, number 3, pages 80–90, May–June 2002.
3. A. Abu-Issa and S. Quigley, 'Bit-swapping LFSR and scan-chain ordering: A novel technique for peak- and average-power reduction in scan-based BIST,' IEEE Transaction Computer-Aided Design Integrated Circuits System, volume 28, number 5, pages 755–759, May 2009.
4. P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, J. Figueras, S. Manich, P. Teixeira, and M. Santos, 'Low-energy BIST design: Impact of the LFSR TPG parameters on the weighted switching activity,' in Proceedings of IEEE International Symposium of Circuits and Systems, volume 1, July 1999, pages 110–113.
5. S. Wang and S. Gupta, 'DS-LFSR: A BIST TPG for low switching activity,' IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems, volume 21, number 7, pages 842–851, July 2002.
6. F. Corno, M. Rebaudengo, M. Reorda, G. Squillero, and M. Violante, 'Low power BIST via non -linear hybrid cellular automata,' in Proceedings of 18th IEEE VLSI Test Symposium, April –May 2000, pages 29–34.
7. P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, and H. Wunderlich, 'A modified clock scheme for a low power BIST test pattern generator,' in Proceedings of 19th IEEE VTS VLSI Test Symposium, March–April 2001, pages 306–311.
8. D. Gizopoulos, N. Krantitis, A. Paschalis, M. Psarakis, and Y. Zorian, 'Low power/energy BIST scheme for datapaths,' in Proceedings of 18th IEEE VLSI Test Symposium, April–May 2000, pages 23–28.
9. Y. Bonhomme, P. Girard, L. Guiller, C. Landrault, and S. Pravossoudovitch, 'A gated clock scheme for low power scan testing of logic ICs or embedded cores,' in Proceedings of 10th Asian Test Symposium, November 2001, pages 253–258.
10. C. Laoudias and D. Nikolos, 'A new test pattern generator for high defect coverage in a BIST environment,' in Proceedings of 14th ACM Great Lakes Symposium VLSI, April 2004, pages 417–420.
11. S. Bhunia, H. Mahmoodi, D. Ghosh, S. Mukhopadhyay, and K. Roy, 'Low-power scan design using first-level supply gating,' IEEE Transaction Very Large Scale Integrated (VLSI) Systems, volume 13, number 3, pages 384–395, Mar. 2005.
12. X. Kavousianos, D. Bakalis, and D. Nikolos, 'Efficient partial scan cell gating for low-power scan-based testing,' ACM Transaction on Design Automation Electronic Systems, volume 14, number 2, pages 28-1–28-15, Mar. 2009.
13. P. Girard, L. Guiller, C. Landrault, and S. Pravossoudovitch, 'A test vector inhibiting technique for low energy BIST design', Proceedings of 17th IEEE VLSI Test Symposium, April 1999, pages 407–412.