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A Strategy to Accelerate VLSI Various Leveled Physical Structure in Floor Planning

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Abstract

With the fast increment in size and unpredictability of VLSI, it is difficult to meet speed and quality necessity of IC physical structure. In this study, we have presented an effective model for brisk floor planning in VLSI top-down various leveled physical structure stream utilizing the active-logic reduction technology. The disentangled show replaces some unique modules in netlist record with filling units which have no sensible associations. This technique can successfully decrease interior coherent units and rapidly foresee if chip configuration accomplishes timing conclusion after best and squares execution with this floorplan to rapidly pass judgment on the floorplan's quality. Most significantly, it can keep up plan quality while accelerating configuration stream. The consequences of six investigations demonstrate that the technique can radically decrease runtime by 6.2 occasions and memory by 2.8 occasions all things considered in VLSI various leveled physical plans.

Keywords:*Active-Logic Reduction Technology, Floor arranging, Hierarchical physical design, VLSI*

INTRODUCTION

The IC physical structure is a procedure of entryway level netlist,amalgamation, floorplanning, control arranging, position, pre route(Fundamentally is trail course), CTS, steering lastly making GDSII format record.Floor arranging is essential in physical structure, it chooses the aftereffects of position and directing (P&R). With the propelled assembling process, expanding chip coordination and littler size, likewise with the presence of Nano scale VLSI plan, VLSI configuration turns out to be progressively needy upon EDA devices with high caliber and productivity [1,2]. In floor arranging stage, the perplexing netlist for the most part contains many millions entryway level units, R. often proposed programmed floorplan strategy in 1982. It is troublesome for EDA apparatuses to finish floor arranging and P&R rapidly and precisely, so EDA devices need a few imperatives for floor arranging. Through various cycles and rehashed alteration of floor planning as per the consequences of P&R, to at long last completion physical structure and meet plan prerequisites. Moreover, numerous new calculations and systems are connected to VLSI floor arranging, for example, reenacted toughening calculation in, guided steady floorplan calculation to proficiently lessen the IR-drop infringement with the B*-tree portrayal in and another P/G system and floor plan strategy for quick structure union in.

Notwithstanding, it is wasteful to invest a great deal of energy with rehashed cycles change, hence it is pressing to figure out how to lessen floor arranging or assessment runtime utilizing propelled calculations and model advancement to accelerate ASIC physical structure, yet additionally keep up floor arranging's

quality [3,4].

QUICK FLOOR PLANNING METHOD

Physical Design Process

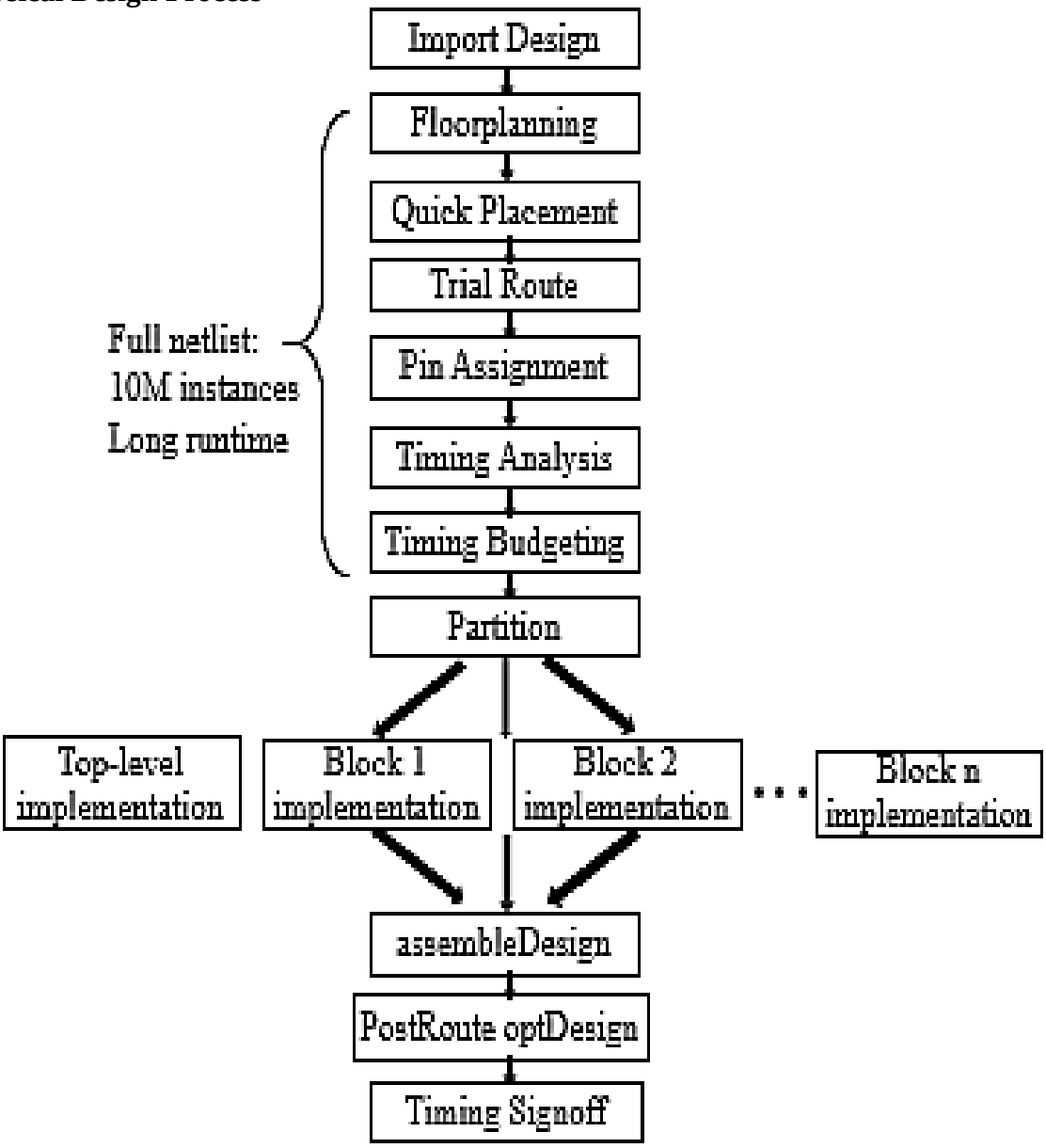

Figure 1: *Traditional hierarchical design.*

To take care of the issue of the expanding VLSI structure multifaceted nature, progressive plan technique is broadly utilized. In this study, the proposed technique is to apply improved model with various leveled plan strategy together to accelerate floor planning and the entire stream. speedy arrangement, 3h for preliminary course, 3h for timing investigation, 10h for timing spending plan, and afterward parcel, square execution and best usage, amass and improvement before timing signoff, at long last the runtime of this strategy was more than 26h [5, 6]. The conventional progressive structure process is appeared in Fig. 1, a 10M plan need 10h for On the off chance that embracing proposed strategy in progressive structure as appeared in Fig. 2, albeit demonstrate creation took 5h, it could drastically spare run time of the following arrangement of procedures, for instance the speedy position took 2h and timing spending plan took 1h, so the entire stream runtime

could be altogether decreased with the proposed technique [7].

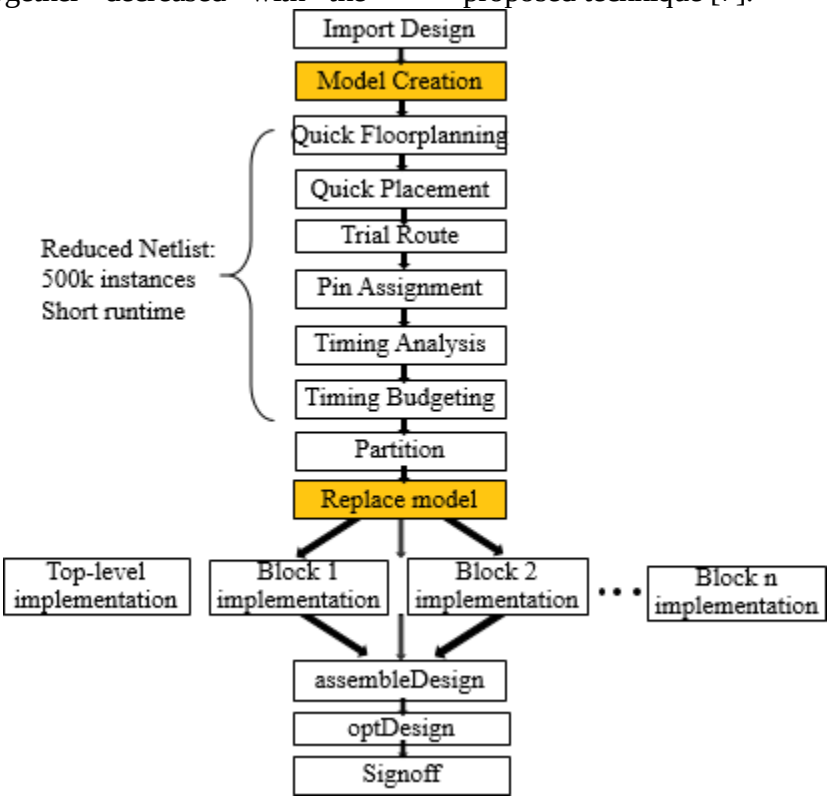

Figure 2: *Hierarchical design of proposed method.*

ACTIVE-LOGICREDUCTION TECHNOLOGY (ART)

Dynamic rationale decrease innovation (ART),utilize the idea of logical reduction in software engineering, alludes to remain the related sensible units when robotization figuring, it will cover the part which is unessential to computation and produce a functioning intelligent view for

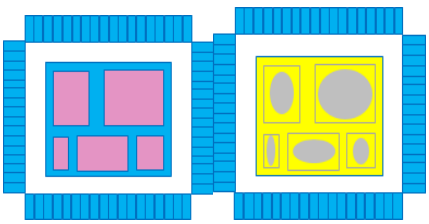

Figure 3: *Diagram of ART technology.*

PC to just observe the dynamic rationale units in this view [8]. Indeed, it is only a functioning sensible view that all unique rationale units stay in structure really. Computer actualizes structure improvement in the dynamic coherent view, and afterward maps the changed parts to the first view, yet not changing inert rationale units which is irrelative with figuring. So, in the way we can lessen invalid estimation to improve computation productivity and decrease runtime. The rule of ART innovation in this study is appeared in Fig. 3. The left diagram demonstrates a whole module in conventional various leveled plan whose rationales in the segment are not obvious, so it just can get limit port definition and data. We know plan improvement depends on timing expectation, for example, yield delay, however the planning forecast is finished before segment, its qualities will veer off from real planning qualities. So, it will require a lot of investment for numerous cycles to accomplish time conclusion through remedying the deviation among dividing and gathering. The correct figure utilizes ART innovation, which can demonstrate the obvious interface rationale part in parcel limit, likewise can recognize the interface legitimate way, the inner rationale and circle way as indicated by their planning

data. At that point use ART innovation to veil dormant rationale ways that are immaterial to calculation, and stay dynamic rationale interface rationales that are applicable to calculation. In this strategy, the planning expectation is nearer to the real world, so it can decrease the runtime of emphases improvement [9].

SIMPLIFIED MODEL AND FLEX FILLER

Rationale minimization calculations has been utilized in VLSI amalgamation, it is a vital advance forward in programmed rationale blend. Speedy floor planning strategy in various leveled physical structure stream can adequately lessen configuration measure by decreasing unimportant rationales, to rapidly foresee plan execution. filling units named flex filler and produce another decreased netlist document that is progressively helpful for brisk floor planning.

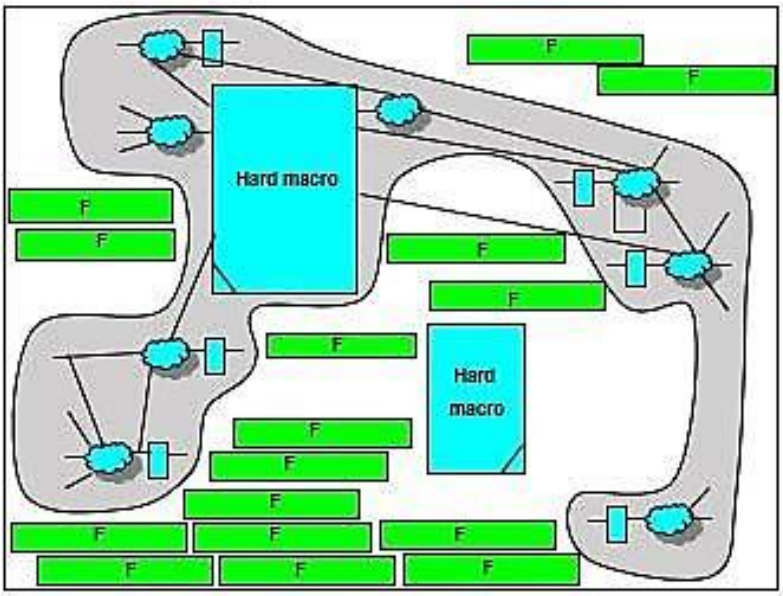

Figure 4: *Schematic diagram of simplified model.*

As appeared in Fig: 4, the improved model the center of this strategy is streamlined model, which is a rough model dependent on ART innovation to supplant full netlist with a producing decreased netlist. Due to floor planning give more consideration to interface associations as opposed to inner rationales, rearranged show expects to evacuate interior immaterial units of modules. At that point supplant it with uses ART innovation to supplant the inward unimportant sensible units with flex fillers in netlist and just stay a few rationales between hard macros and modules. In this manner, the diminished netlist just contains related interface rationales, it is not just lessen data in netlist to accelerate plan yet in addition not debilitate floor planning's quality. By and large to lessen about 90% of configuration measure is the best simplified model removes internal inactive logic, mainly is regret logical units. Flex fillers as alternative units are the special units which simulate the location and area of removed logical units to remain original utilization and area for more accurate floor planning.Firstly, a flex filler's territory is handfuls bigger than standard modules, so it can moderately diminish the quantity of modules in netlist to lessen configuration scale by rearranging inside rationales. Also, flex filler itself does not have any sensible association, so P&R don't need to consider their associations which can spare runtime. Additionally, floor arranging should modify by aftereffects of P&R, so the decrease will accelerate timing

investigation and assessment of floor planning while at the same time diminishing P&R run time, at long last by and large floor arranging runtime can be diminished to an expansive degree. Fig. 5 demonstrates the flex fillers in EDA instrument's physical view, chose rectangular box is flex filler whose estimate is a lot bigger than the kept up interface rationales in lower left corner of Fig. 5.

Figure 5: *Flex filler of physical view in EDA tool.*

EXPERIMENTAL RESULT AND ANALYSIS

This study was actualized on Cadence Inc's EDA physical plan programming "Innovus"(the unique name is Encounter), investigated a 2.1M car electronic chip structure and 5 other chips. Fig. 6 is the chip with no physical structure. The streamlined model dependent on ART innovation is a physical dimension recreation show with decreased netlist, supplant dormant rationales with flex fillers and stay dynamic rationales.

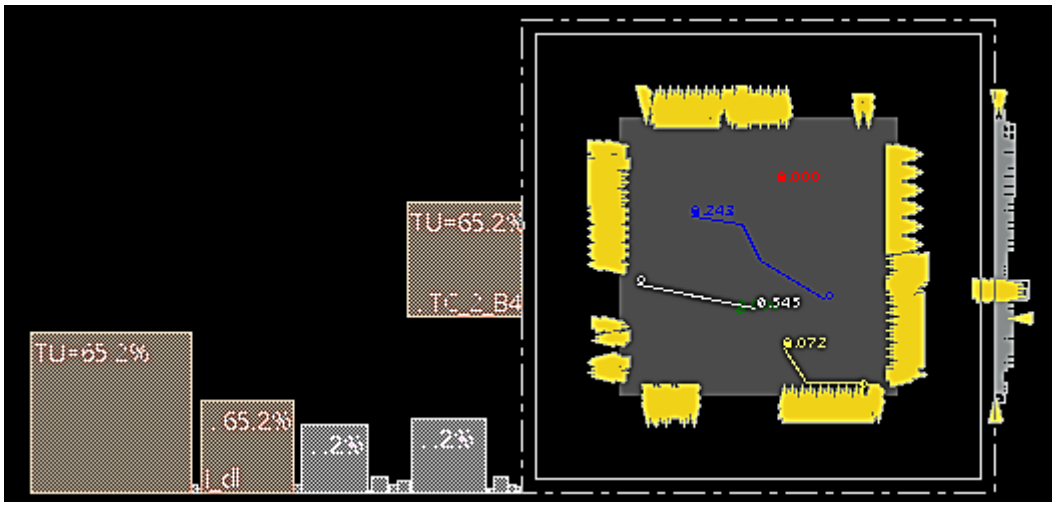

Figure 6: *Initial chip without physical design.*

The experiment defined 89 modules as simplified models and gave a detailed model creation report in Fig. 7. The initial instances is 2086769, about 2.1M, after modeling, it declined 128695+71829=0.2M, so this method reduced design size from 2.1M to 0.2M, decreasing to 9.6% of original netlist. With reduced netlist, quick floor planning method was easier to implement timing

analysis, quick placement, preroute, optimization and budgeting. To prove it, we recorded the run time of each step before partition step in hierarchical design flow and compared the run time between design flow without model and with model. As shown in Table 1, without simplified model, total flow run time before partition step was 807.95 minutes, but with simplified model, total flow run time before partition step was 145.08 minutes. So run time reduced by 5.57 times, and peak memory decreased by 2.22 times from 20G to 9G. Besides, in Fig. 8, it is the chip floor planning result with simplified model, and the simplified models was marked with colored squares.Actually, the method not only can dramatically speed up hierarchical physical design flow, it would also keep good timing and congestion results on one-pass flow. In Table 2, it used RC extraction engine to report timing after assembling design, there were all 6.87e+05 paths, and we focused on worst negative slack (WNS) of "reg2reg" -0.048ns, which was reasonable for one-pass flow when we evaluated design's time closure. The congestion reports showed the overall horizontal congestion was 0.10% and vertical congestion was 0.35%, which was acceptable in a 2.1M design [10, 11].

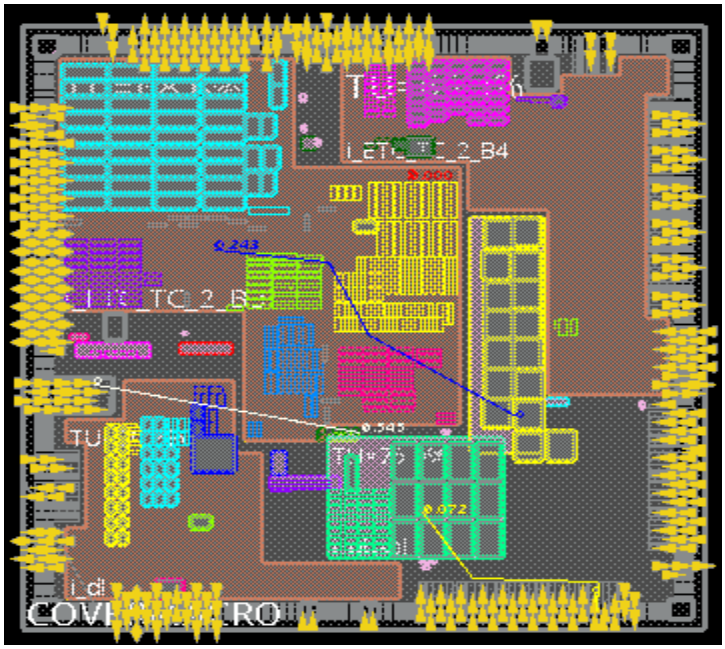

Figure 7: *Chip design result of floor planning. With simplified model.*

Table 1: *Timing report after assembling design.*

Setup mode	All	reg2reg	Default
WNS(ns)	-0.050	-0.048	-0.050
TNS(ns)	-2.912	-1.300	-1.612
Violatingpath	311	149	162
All paths	6.87e+05	6.86e+05	432

So, as to additionally check the adequacy of proposed strategy, we probed a few diverse gigantic size of structures to look at customary technique and proposed strategy in various leveled physical plan stream. In Table 2, the snappy floor planningtechnique improve runtime by 6.2 occasions and decrease memory by 2.8 occasions overall. It gives the establishment to smooth usage of P&R in various leveled physical plan and

improve the execution of EDA instrument in VLSI physical structure.

Table 2: *Different designs using the proposed and traditional method flow comparison.*

No.	Designsize	Runtimeimprovement	Memoryreduction
1	2.1M	5.6	2.2
2	2.2M	3.9	2.0
3	2.6M	5.2	2.6
4	2.8M	5.4	2.3
5	3.5M	7.2	3.2
6	8.8M	9.7	4.3
Average		6.2	2.8

CONCLUSION

With the fast increment in size and unpredictability of VLSI, EDA apparatuses are utilized in progressively successful approach to meet speed and quality necessity of IC chip plan. Floor arranging is the reason for P&R in physical structure, yet it ordinarily represents around 33% run time in entire stream to locate an appropriate floor plan, so shortening the floor arranging and assessment run time is a powerful method to accelerate chip's physical structure. Utilizing the legitimate decrease technique to make demonstrate for floor arranging in best down various leveled physical plan stream can adequately diminish configuration estimate by lessening immaterial data of this progression in netlist, at that point it can rapidly foresee if configuration meets timing and clog necessity after physical structure execution. It demonstrated the strategy can radically diminish the run time by 6.2 occasions and memory by 2.8 occasions by and large in VLSI various leveled physical structures as per the six correlation tests.

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