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Compensating Threshold Voltage Roll-Off in Nanoscale MOSFET with Parameter Adjustment

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Abstract

During last few decades, the Silicon-On-Insulator (SOI) technology has been identified as a possible solution for reducing constrains over transistor miniaturization and to maintain continuous progress in semiconductor chip design industry. The SOI CMOS has numerous advantages over conventional bulk CMOS technology but it is not fully immune of several short channel effects. One of the primary impacts of short channel effects in SOI MOSFET is the degradation of device threshold voltage with decreasing channel length. Such threshold voltage degradation factor with reducing channel length is normally known as threshold voltage roll-off which restricts further scaling of SOI devices. But such roll-off factor can be adjusted by fine tuning the other structural parameters and this fact has been established with theoretical modeling and subsequent simulation under this present work. Under present analysis, a two dimensional generalized analytical threshold voltage model has been presented for nanoscale SOI MOSFET. Threshold voltage performance has been simulated and analyzed for various structural parameters e.g.; channel length, channel doping concentration, gate oxide thickness etc. Finally, how much fine tuning is required for various structural parameters (channel doping concentration and gate oxide thickness) to compensate threshold voltage roll-off factor at various channel length, has been calculated. The simulation results have shown that the unavoidable threshold voltage roll-off effect associated with technology scaling can be minimized by fine-tuning other device parameters.

Keywords: *SOI MOSFETs, short channel effect, surface potential, threshold voltage*

INTRODUCTION

From the beginning the microelectronics industry has followed Moore's law, doubling processing power every 18 months and such performance improvement has been achieved by device scaling [1]. As scaling of planar CMOS has been facing significant challenges, several nonconventional geometry structures have been studied experimentally as well as theoretically [1, 2]. Among the nonconventional structures, Silicon-On-Insulator (SOI) structure has received much attention of researchers around the globe because of its inherent functional advantages [3]. The SOI technology offers many advantages over conventional MOS technology such as higher speed, lower power dissipation, high radiation tolerance, lower parasitic capacitance and lower Short Channel Effects (SCEs) etc. The SOI technology is also manufacturing compatible with the existing bulk silicon CMOS technology [4]. Although SOI shows superior performance over its bulk counterpart, it is not fully immune to various SCEs [3, 4]. Among those SCEs related impact the reduction of threshold voltage with decreasing channel length, Threshold Voltage Roll-off (TVR), is considered to be the most serious and challenging problem with submicron or nanometer SOI technology [5]. To encounter this problem numerous theoretical and experimental researches have been carried out in recent past [6]. Such theoretically and experimentally proposed schemes include gate metal stack layers, dual and multiple material gates, metal interfacial layer with metal electrode etc. [6]. But till now, the ultimate goal of achieving threshold voltage control for ultra low dimensional SOI structures has not been partially archived [7].

Under this present theoretical analysis the reduction of TVR factor has been suggested with fine tuning of other device parameters. Firstly, a generalized two dimensional analytical threshold voltage model based on the Poisson's equation solution has been derived for a uniformly doped nanoscale SOI MOSFET. The effect of the junction induced two dimensional field effect is incorporated in the present analytical model. The threshold performance of the nanoscale SOI is investigated with structural parameter variations and simulated results are presented along with technical discussions. Finally, for different channel lengths, the tuning factors for various device parameters (channel doping concentration and gate oxide thickness) to eliminate TVR, are calculated and

presented.

Analytical SOI Model

In a nanoscale SOI device, potential profiles in the channel will be two-dimensional in nature [8]. A generalized layered structure of a SOI MOSFET is as shown in Figure 1.

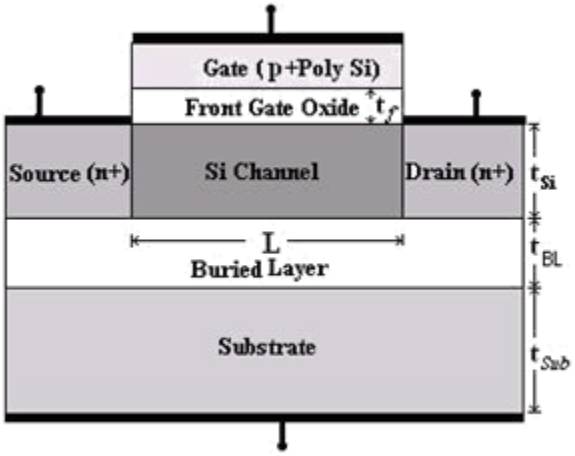

Fig. 1: *Cross Sectional View of an SOI MOSFET.*

The 2-D Poisson's equation in the two-dimensional channel region of the depleted silicon film body ($0 \le x \le L$, $0 \le y \le t_{si}$) can be written as [9, 10]

$$\frac{\partial \xi(x,y)}{\partial x^2} + \frac{\partial \xi(x,y)}{\partial y^2} = \frac{qN_a}{\varepsilon_{Si}} \quad (1)$$

Where, $\xi(x, y)$ is the 2-D potential profile in the silicon channel, N_a is the doping concentration of the p-type channel and the substrate and ε_{Si} is the permittivity of silicon. Considering a second order potential approximation, the 2D potential profile in the channel is written as [9];

$\Xi(x, y) = P_1(x) + P_2(x)\, y + P_3(x)\, y2$ (2)

Where P_1, P_2, P_3 all are functions of *x* and solved for boundary conditions (at $t_{Si}=0$ and $t_{Si}=t_{Si}$) according to the continuity of electrostatic potential and Gauss's law as [9];

$$P_1(x) = \xi_{sf}(x) \quad (3)$$

$$P_2(x) = -\frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{V_{gs}^{'} - \xi_{sf}(x)}{t_f} = -\frac{c_f}{\varepsilon_{Si}} [V_{gs}^{'} - \xi_{sf}(x)] \quad (4)$$

$$P_3(x) = \frac{c_{BL/air} \left\{ V_{ss}^{'} + V_{gs}^{'} [\frac{c_f}{c_{BL/air}} + \frac{c_f}{c_{BL/air}}] - \xi_{sf}(x)[1 + \frac{c_f}{c_{BL/air}} + \frac{c_f}{c_{BL/air}}] \right\}}{t_{Si}^2 [c_{BL/air} + 2c_f]} \quad (5)$$

Where; $\xi_{sf}(x)$ is the front surface potential, $V_{gs}^{'}$ and $V_{ss}^{'}$ are the effective applied front and back channel voltages given as $V_{gs}^{'} = V_{gs} - V_{ffb}$ and $V_{ss}^{'} = V_{ss} - V_{bfb}$. The V_{ffb} and V_{bfb} are the front and back channel flat band voltages, respectively. The C_f and C_{BL} are taken as front and buried oxide layer capacitances per unit area. The ε_{ox} and ε_{Si} are the dielectric constants of the front oxide and silicon respectively. Now

inserting equations 3 to 5 into the equation 2, the expression for 2-D potential profile in the channel region will be formed. Finally solving equation 1 with equation 2, considering source-channel and channel-drain boundary conditions ($\xi(x=0, y=0)=V_{bi}$ and $\xi(x=L, y=0)=V_{bi}+V_{DS}$) the final expression of surface potential will be formed [6, 7].

$$\xi_{sf} = 2\sqrt{AB} - \frac{k3}{k2} \quad (6)$$

Where,

$$A = s1 + (k3/2k2), \qquad B = s2 + (k3/2)$$

$$s1 = \frac{Vbi\left(\sqrt{k2}\right)L + Vds}{2\left(\sqrt{k2}\right)L}, \qquad s2 = \frac{Vbi\left(\sqrt{k2}\right)L - Vds}{2\left(\sqrt{k2}\right)L}$$

$$k1 = 1\,,\ k2 = -\frac{cf}{\epsilon si},\ k3 = -\frac{C_{BL}\,Vss'}{t_{si}\,\epsilon_{si}} - \frac{qNA}{\epsilon_{si}} + \frac{cf\,Vg's}{\epsilon_{si}}$$

Where, the V_{bi} is the build-in-potential of p-type silicon channel. Using the condition for minimum surface potential $\frac{d\xi_{sf}(x)}{dx} = 0$, the minimum surface potential point has been obtained as [9],

$$x_{(min)} = \frac{1}{2}\sqrt{\frac{k1}{k2}}\ln\left(\frac{B}{A}\right) \quad (7)$$

Using X_{min}, the minimum front surface potential ($\xi_{sf,\,min}$) has been calculated as;

$$\xi_{sf(min)} = 2\left[\sqrt{s1s2} + \frac{\left(\sqrt{s1s2}\right)k3}{4s2k2} + \frac{k3\sqrt{s1s2}}{4s1k2}\right] - \frac{k3}{k2} \quad (8)$$

Finally the threshold voltage expression has been calculated from eqn. 8, by considering strong inversion condition; $Vth = V_{gs}$ when $\xi sf,\ min = 2V_{bi}$.

$$Vth = \frac{\epsilon_{si}}{cf}\left[\frac{8s1s2\left(Vbi - \sqrt{s1s2}\right)}{\sqrt{s1s2} - 4s1s2} + \frac{C_{BL}V'ss}{t_{si}\,\epsilon_{si}} + \frac{qNa}{\epsilon_{si}}\right] + V_{ffb} \quad (9)$$

SIMULATED RESULTS

The various parameter values which are used for calculation and simulation purpose are given in Table 1.

Table 1: *Value of Various Parameters.*

Parameter	Symbol	Value
Gate Oxide Thickness	t_f,	7 nm
Channel Thickness	t_{Si}	50 nm
Buried Layer Thickness	t_{air}	100 nm
Channel Length	L	100 nm
Source/Drain Doping Conc.	N_d	$1*10^{23}/m^2$
Channel Doping Conc.	Na	$1*10^{21}/m^2$
Intrinsic Carrier Conc.	N_i	$1*10^{16}/m^2$

Any deviation in parameter value from their default value (as given in the Table above), has been mentioned in the figure caption of the corresponding figure.

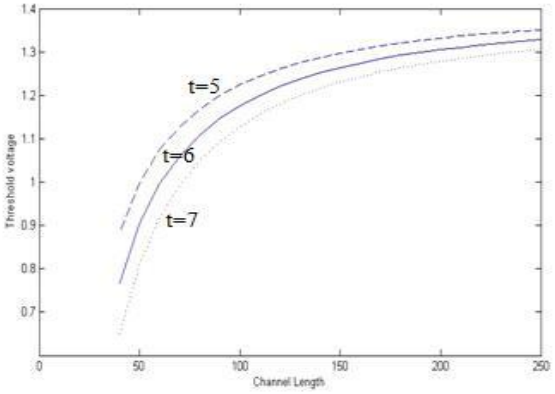

Fig. 2: *TVR with Decreasing Channel Length (in nm) for Various Gate Oxide Thicknesses (t in nm).*

Threshold voltage decreases with decrease in effective channel length due to enhanced short channel effects and is referred as the threshold voltage roll-off as shown in Figure 2.

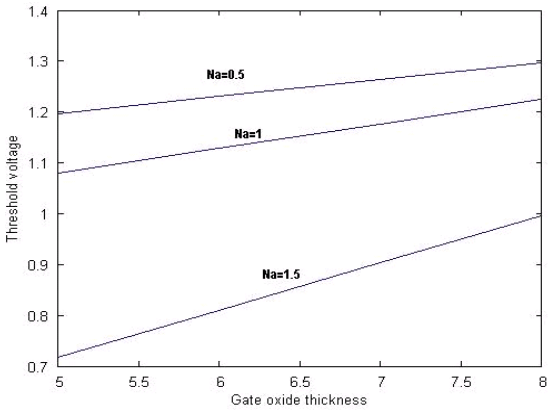

Fig. 3: *Variation in Threshold Voltage with Variations in Gate Oxide Thickness for Na: 0.5,1 and 1.5 (×$10^{21}/m^2$).*

As shown in the Figure 3, the threshold voltage increases with an increase in gate oxide thickness the short- and long-channel devices due to the reduced control of the front gate voltage over the channel [9, 10].

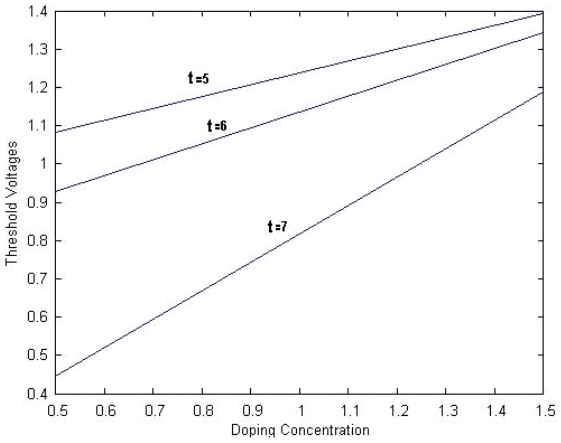

Fig. 4: *Variation in Threshold Voltage with Variations in Channel Doping Concentration (In $10^{21}/M^2$) for Gate Oxide Thickness; 5, 6 and 7 nm.*

Threshold voltage variation with channel doping concentration is plotted in Figure 4. The threshold voltage increases with channel doping concentration because the channel becomes more p-type and thus higher gate voltage is required to create inversion [9, 10].

Table 2: *Value of Various Parameters.*

Channel Length(L)	**TVR Factor (V)**	**Changing Na(×$10^{21}/m^2$)**	**TVR Compensated (V)**	**Gate Oxide Thickness (nm)** t_i	**TVR Compensated (V)**	**Total TVR Compensated (V)**
50 nm	0.4	1 →0.6	0.3	7→5	0.1	(0.3+0.1=) 0.4
100 nm	0.12	1→0.8	0.09	7→6	0.04	(0.09+0.04=) 0.12
150 nm	0.03	1→0.92	0.02	7→6.8	0.01	(0.02+0.01=) 0.03

The TVR factor is calculated as the deviation of threshold voltage from its flat

bulk value due to reduced channel length. The TVR factors at various channel length and corresponding simultaneous Na and t_f tuning factors to compensate TVR factors, are shown in the Table 2.

CONCLUSION

Under the present analysis, a two dimensional generalized threshold voltage model for nanoscale SOI MOSFETs has been developed and analytical expressions for threshold voltage has been derived. The short channel threshold performance of the device with different parameter variations has been studied. Effects of the variation of different parameters, such as channel length, gate oxide thickness and channel doping concentration, on the threshold voltage are simulated and results are analyzed to understand their comparative impact over TVR factor. Finally, the tuning factors for various parameters to compensate TVR factors for different channel lengths are calculated. Present analysis predicts that such idea of parameter tuning will be able to minimize threshold voltage roll off factor and thus will facilitate further downscaling of devices.

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