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Improvements in the Design of Low-voltage Low-Power Double Tail Comparator

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Abstract

The circuit of a standard double-tail comparator is changed for low-power and quick operation even in little provides voltages. While not complicating the planning and by adding few transistors, the feedback throughout the regeneration is reinforced, which ends up in remarkably reduced delay time. Post-layout simulation leads to a 0.18-μm CMOS technology ensure the analysis results. It is shown that within the planned dynamic comparator each the facility consumption and delay time are considerably reduced. The most clock frequency of the planned comparator may be enhanced to 2.5 and 1.1 GHz at provide voltages of 1.2 and 0.6 V, whereas, overwhelming 1.4 mW and 153 μW, severally. The quality deviation of the input-referred offset is 7.8 mV at 1.2 V supply.

Keywords*: double-tail comparator, dynamic clocked comparators, low power analog design*

INTRODUCTION

Comparator is one among the basic building blocks in most analog-to-digital converters (ADCs). Several high speed ADCs, admire flash ADCs, need high-speed, low power comparators with little chip space. High-speed comparators in ultra-deep sub-micrometer (UDSM) CMOS technologies suffer from low provide voltages particularly once considering the actual fact that threshold voltages of the devices have not been scaled at identical pace because provide voltages of the trendy CMOS processes [1–3]. Hence, planning high-speed comparators is tougher once the availability voltage is smaller. In different words, during a given technology, to attain high speed, larger transistors square measure needed to compensate the reduction of provide voltage that additionally implies that a lot of die space and power is required. Here, a comprehensive analysis concerning the

delay of dynamic comparators has been conferred for numerous architectures. What is more, supported the double-tail structure planned, a brand new dynamic comparator is conferred, that does not need boosted voltage or stacking of too several transistors [4, 5]. Simply by adding a number of minimum-size transistors to the standard double-tail dynamic comparator, latch delay time is deeply reduced. This modification conjointly leads to appreciable power savings compared to the standard dynamic comparator and double-tail comparator.

DESIGN

Figure 1 demonstrates the schematic diagram of the proposed dynamic double-tail comparator. Due to the better performance of double-tail architecture in low-voltage applications, the proposed comparator is designed based on the double-tail structure. The main idea of the proposed comparator is to increase ΔVfn/fp in order to increase the latch regeneration speed. For this purpose, two control transistors (Mc1 andMc2) have been added to the first stage in parallel to M3/M4transistors but in a cross-coupled manner [6, 7].

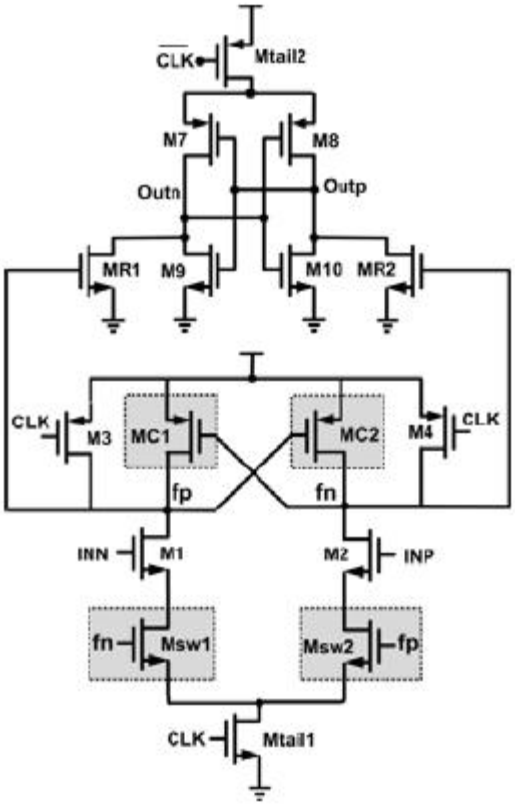

Fig. 1: *Schematic Diagram of Proposed System.*

During operation, in the reset phase (CLK = 0, M_{tail1} and M_{tail2} are off, avoiding static power), M_3 and M_4 pulls both f_n and f_p nodes to V_{DD}, hence transistor M_{c1} and M_{c2} are cut off. Intermediate stage transistors, M_{R1} and M_{R2}, reset both latch outputs to ground. During decision-making phase (CLK = V_{DD}, M_{tail1}, and M_{tail2} are on), transistors M_3 and M_4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since f_n and f_p are about V_{DD}). Thus, f_n and f_p start to drop with different rates according to the input voltages. Suppose $V_{INP} > V_{INN}$, thus f_n drops faster than f_p,

(since M_2 provides more current than M_1). As long as f_n continues falling, the corresponding pMOS control transistor (M_{c1} in this case) starts to turn on, pulling f_p node back to the V_{DD}; so another control transistor (M_{c2}) remains off, allowing fn to be discharged completely. In other words, unlike conventional double-tail dynamic comparator, in which ΔVfn/fp is just a function of input transistor transconductance and input voltage difference, in the proposed structure as soon as the comparator detects that for instance node fn discharges faster, a pMOS transistor(M_{c1}) turns on, pulling the other node fp back to the V_{DD} [8, 9].

Therefore, by the time passes, the difference between f_n and f_p (ΔVfn/fp) increases in an exponential manner, leading to the reduction of latch regeneration time. Despite the effectiveness of the proposed idea, one of the points which should be considered is that in this circuit, when one of the control transistors (e.g., M_{c1}) turns on, a current from V_{DD} is drawn to the ground via input and tail-transistor (e.g., M_{c1}, M_1, and M_{tail1}), resulting in static power consumption. To overcome this issue, two nMOS switches are used below the input transistors (M_{sw1} and M_{sw2}, as shown in Figure 2).

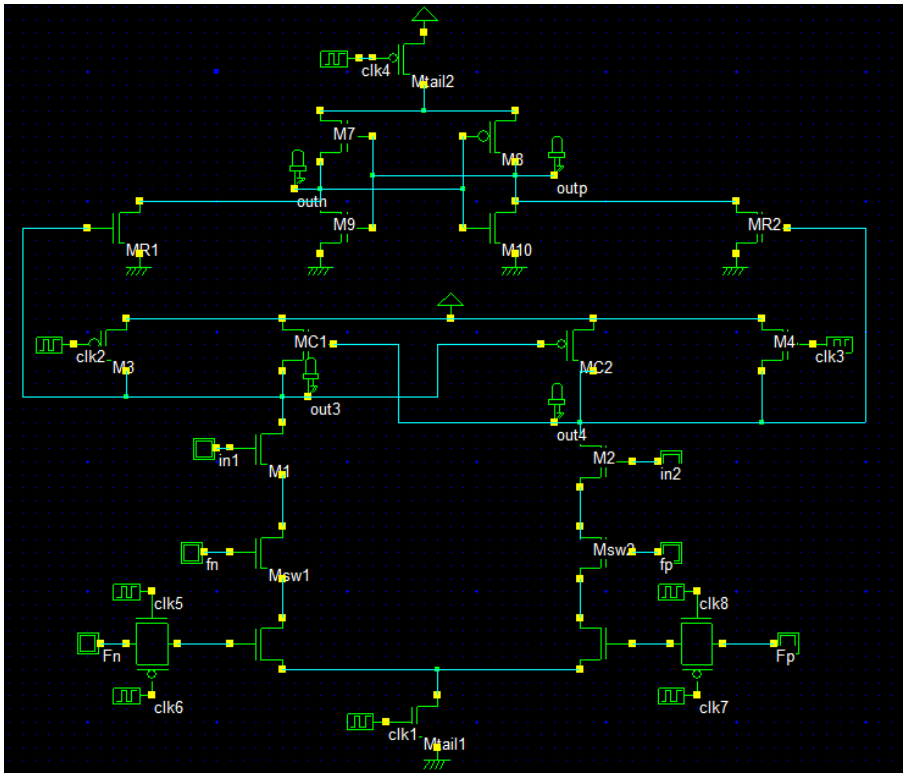

Fig. 2: *Modified Circuit Schematic Diagram.*

Delay Analysis

Enhancing ΔV_0

We outline t0, as a time when that latch regeneration starts. In alternative words, t0 is taken into account to be the time it takes (while each latch outputs area unit rising with completely different rates) till the primary nMOS semiconductor device of the consecutive inverters activates, in order that can pull down one in every of the outputs and regeneration will begin. Consistent with (2), the latch output voltage distinction at time t0, (ΔV0) includes a respectable impact on the latch regeneration time, specified larger ΔV0 ends up in less regeneration time.

Effects of Enhancing Latch Effective Transconductances

In conventional double-tail comparator, both f_n and f_p nodes will be finally discharged completely. In our proposed comparator, however, the fact that one of the first stage output nodes (fn/fp) will charge up back to the V_{DD} at the beginning of the decision making phase, will turn on one of the intermediate stage transistors, thus, the effective.

Reducing the Energy per Comparison

It is not solely the delay parameter that is improved within the changed projected comparator, however, the energy per conversion is reduced in addition. Earlier, in typical double-tail topology, each fn and fp nodes discharge to the bottom throughout the choice creating section and every time throughout the reset section they must be force up back to the VDD. However, in our projected comparator, just one of the mentioned nodes (fn/fp) has got to be charged throughout the reset section.

Design Considerations

In designing the proposed comparator, some design issues must be considered. When determining the size of tail transistors (*M*tail1 and *M*tail2), it is necessary to ensure that the time it takes that one of the control transistors turns on must be smaller than *t*0 (start of regeneration).

$$ton, Mc1(2) \rightarrow \frac{|VThp.CL.fn(p)|}{In1,2} < \frac{VThnCLout}{IB1}$$

$$\rightarrow \frac{|VThp.CL.fn(p)|}{\frac{Itail1}{2}} < \frac{VThnCLout}{\frac{Itail2}{2}}$$

RESULT DISCUSSION

Simulation Results

The post-layout simulation results of the delay and the energy per conversion of the mentioned dynamic comparators versus supply voltage variation. As shown in Figure 3 Voltage vs. Current, the delay of

the proposed double tail dynamic comparator is significantly reduced in low-voltage supplies. It is obvious that at high supply voltages, all structures have approximately similar performances, about 200ps clock-to-output delay (including clock buffer) with 0.65 pJ/bit conversions for 8-mV offset.

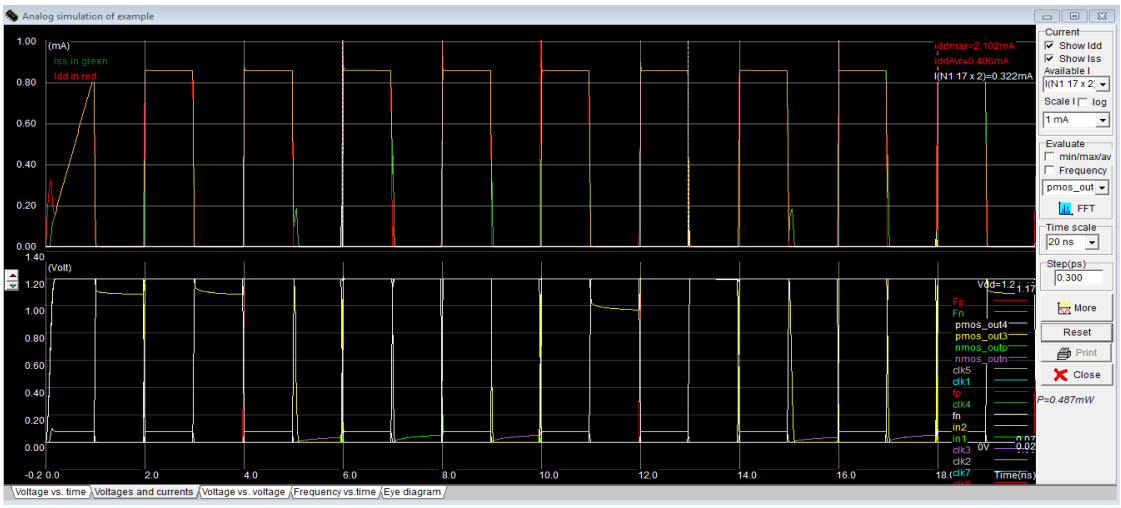

Fig. 3: *Post Layout Simulation Results of Voltage vs. Time.*

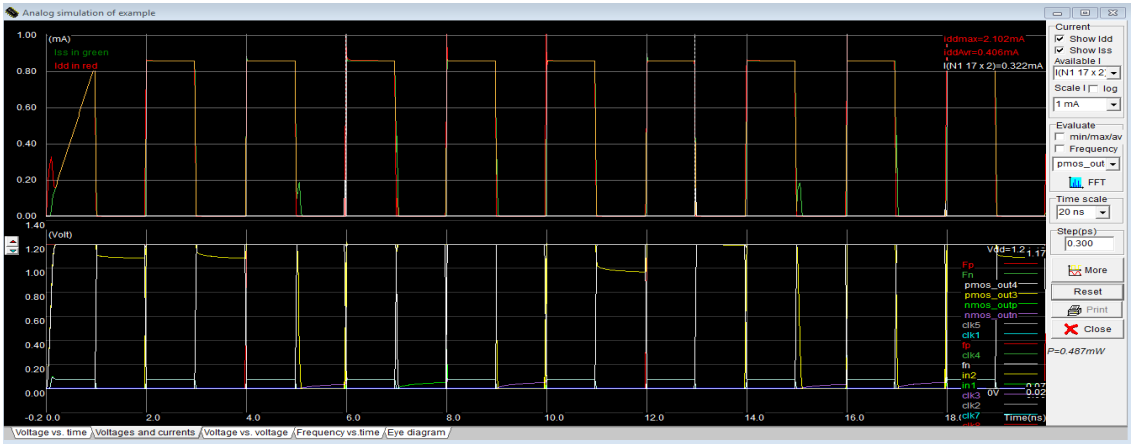

Fig. 4: *Post Layout Simulation Results of Voltage vs. Current.*

CONCLUSION

In this paper, we presented a comprehensive delay analysis for clocked dynamic comparators and expressions were derived. Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were analyzed. Also, based on theoretical analyses, a new dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the

comparator. Post-layout simulation results in 0.18-µm CMOS technology confirmed that the delay and energy per conversion of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator.

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