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Design and Implementation of High Performance Analog CMOS Based Circuits using Pspice: An Overview

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Abstract

Current mirror is that the basic key component in VLSI style. To get high performance analog circuit application, the output electrical resistance and accuracy area unit the foremost vital parameter to work out the performance of this mirror. A brand new current mirror is planned during this paper to produce high accuracy and extremely high output electrical resistance. To increase the output resistivity and matching accuracy considerably a unique feedback gain is employed. The new projected current mirror additionally has output swing similar because the ancient two stage cascode current mirror.

Keywords: *Cascode current mirror, IAFCCM, negative feedback gain, two stage current mirror*

INTRODUCTION

Due to the higher performance the present mode approach is gaining interest additional and additional [1–5]. The decreasing power offer voltage of digital small physics makes it appropriate for mixed mode application is that the reason for victimisation current mode circuit. The present mirror is employed for biasing or loading components in analog circuit style. The foremost vital parameter would not to confirm the performance of current mirror area unit accuracy and output electric resistance. It is often wont to notice several researches that target these two points. To extend the output electric resistance the cascode current mirror and, therefore, the RGC current mirror is employed [6–9]. IAFCCM was planned to extend the accuracy [8]. To attain higher output electric resistance, multi stage cascode mirror has been used, though its suffer from low output voltage swing. The output electric resistance of the two stage cascode current mirror is below the output electric resistance of RGC current mirror

and, therefore, the accuracy of the RGC current mirror is not adequate for prime preciseness application.

The accuracy of IAFCCM is better than RGC current mirror and the output impedance of IAFCCM is equivalent to the RGC current mirror. A new high output impedance current mirror is proposed in the paper to improve the accuracy and the output impedance of the new current mirror, it is based on the RGC circuit. To increase the output impedance and matching accuracy significantly a novel feedback gain stage is used. The new current mirror is similar to the traditional two stage cascode current mirror, so the proposed current mirror is better than that of RGC and IAFCCM.

DESCRIPTION OF PREVIOUS CIRCUITS AND THE NEW CURRENT MIRROR

Previous Current Mirror Circuits

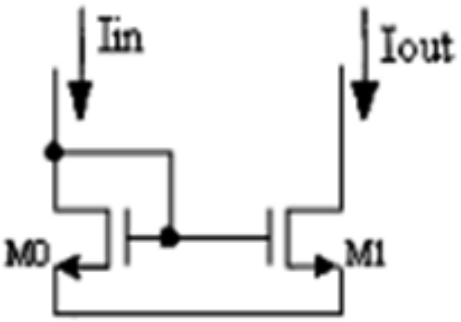

Fig. 1: *Traditional Current Mirror [1].*

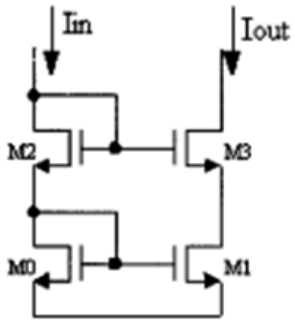

Fig. 2: *Cascode Current Mirror [1].*

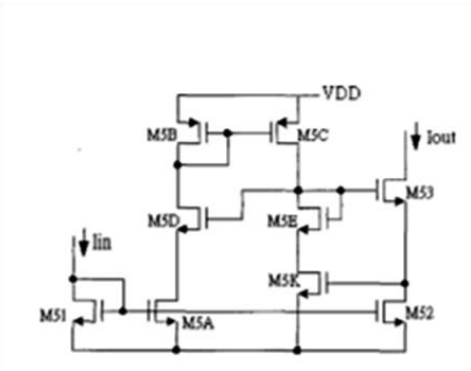

Fig. 3: *IAFCCM [1].*

The traditional current mirror is shown in Figure 1. As the traditional current mirror's output impedance is not infinite, it will influence the output current I_{out} by the variation of the output node voltage V_{ds}. It is a drawback in the analog circuits. In Figure 2 the cascode current mirror is shown. It has the matching accuracy problem and it was proposed to improve the output impedance [7]. In Figure 3 the IAFCCM is shown. It was proposed to increase the output impedance, output voltage swing and matching accuracy. IAFCCM improves lots of output voltage swing, but the output impedance is not

high enough. Meanwhile the output node voltage influences the output current I_{out}.

The Proposed New Current Mirror Circuit

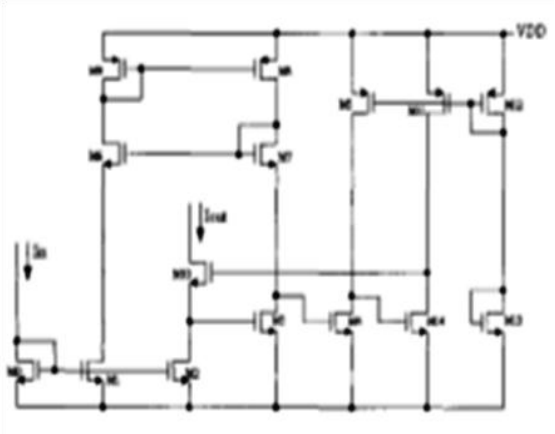

Fig. 4: *The Proposed Current Mirror [1].*

The proposed new current mirror improves the new key parameters of the current mirror, the matching accuracy and output impedance. The Figure 4 shows the schematic diagram of the proposed new current mirror. Here are some MOS transistors such as M0, M2, M10 are used as a two stage cascode current mirror and some MOS transistors such as M1, M6, M9, M7 and M8 are used to improve the matching accuracy of the cascode current mirror. M3, M4 and M14 are the three novel negative feedback gain stages that can increase the output impedance of the current mirror significantly.

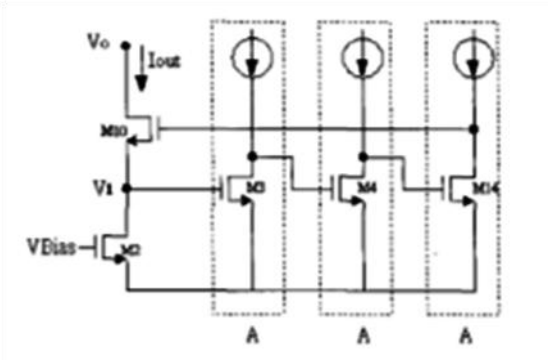

Fig. 5: *The Feedback Circuit [1].*

The feedback circuit of the current mirror is shown in Figure 5 and the voltage gain of each gain stage is shown as A. The output impedance is out of the new proposed current mirror can be estimated by following.

$$V_1 = = i \frac{1}{gd_2} \qquad [1]$$

$$i = gm_{10} * (-|A|^3\text{-}1) * V_1 + gd_{10} * (V_0 - V_1) \qquad [2]$$

$$\Rightarrow i * \left(1 + \frac{gm_{10}}{gd_2}|A|^3 + \frac{gm_{10}}{gd_2} + \frac{gd_{10}}{gd_2}\right) = gd_{10} * V_0$$

$$\Rightarrow \frac{V_0}{i} = (1 + \frac{gm_{10}}{gd_2}|A|^3 + \frac{gm_{10}}{gd_2} + \frac{gd_{10}}{gd_2}) \div gd_{10}$$

$$= \frac{gm_{10}}{gd_{10}}|A|^3 \frac{1}{gd_2} \qquad \ldots [3]$$

$$R_0 = \frac{gm_{10}}{gd_{10}} \frac{1}{gd_2}|A|^3 \qquad \ldots [4]$$

As shown in equation (4) where A≅ $-\frac{gm_i}{gd_i}$ (i= 3, 4 and 14 respectively), the proposed new current mirror has much larger R_{out} than that of the IAFCCM which has output impedance

$$R_{out} = gm_{53}gm_{5k} \frac{1}{gd_{52}} \frac{1}{gd_{58}} [\frac{1}{gd_{5k}} // \frac{1}{gd_{5c}}]$$

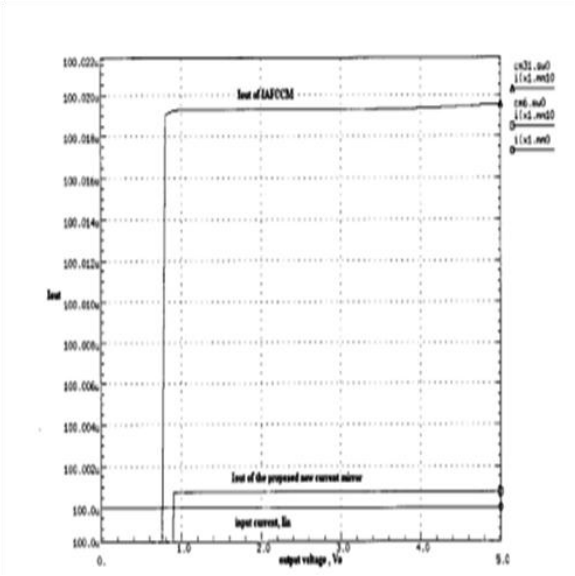

Fig. 6: *The I-V Curve of the Simulation Result [1].*

In Figure 5 the voltage V_1 is independent of V_0. When V_0 and V_1 are increased then the V_{ds14} is decreased due to the three gain stages. The negative feedback signal is created by connecting V_{ds14} to the gate of M_{10}. Therefore, decrease in V_{ds14} decrease the V_1. Thus, the negative feedback loop locks V_1 so that a stable I_{out} is obtained. Now the proposed new current mirror has high output impedance.

For a good current mirror another factor is the matching accuracy between I_{in} and I_{out} [10]. The MOS transistors M_6, M_7, M_8 and M_9 are used to match the current I_{m1} and I_{m2} in the new proposed circuit and further make $V_{Gs3}= V_{Gs1}$. From $V_{Gs1}= V_{Gs0}= V_{Ds0}$ and $V_{Gs3}= V_{Ds2}$, we can find $V_{Ds2}= V_{Ds0}$ which results $I_{in=} I_{out}$. The proposed new current mirror has better matching accuracy than the IAFCCM and it is proved by the HSPICE simulation results.

SIMULATION RESULTS

The HSPICE simulation results are based upon 0.35µm 1P4M CMOS process which has a supply voltage of 3.3V where, L= 1µm for all transistors except M_8, M_9 transistors for which L= 3µm. W= 20µm for M_0, M_1, M_2, M_3, M_6, M_7, M_{10} and

W= 40µm for M_8, M_9 to ensure I_{out}= 100µA

W= 5µm for M_4, M_{14}

W= 10µm for M_5, M_{11}

W= 1µm for M_{12}, M_{13}

The I-V curve simulation result of the proposed new current mirror and IAFCCM is shown in Figure 6. The I-V plot of the input current I_{in} is the lowest line. The top line is the I-V plot of IAFCCM, it shows that the output impedance is not that much high to avoid the influence of V_{ds}, i.e., under the variation of the output voltage V_0 the I_{out} will be changed. The I-V plot of the proposed circuit is the middle line and it indicates that the output impedance of the proposed circuit is higher than IAFCCM. In Figure 6 the comparison results of the accuracy is shown. The proposed circuit has a matching accuracy better than IAFCCM when the input current I_{in}= 100µA.

Table 1: *The Proposed CM Performance Comparison with IAFCCM [1].*

Issue	The proposed circuit	IAFCCM
Mirroring error Iin=5uA	0.016%	0.036%
Mirroring error Iin=10uA	0.012%	0.03%
Mirroring error Iin=100uA	0.001%	0.019%
Mirroring error Iin=200uA	0.005%	0.015%
Mirroring error Iin=300uA	0.012%	0.014%
Mirroring error Iin=400uA	0.026%	0.013%
Rout	$\propto \frac{1}{gd}\left(\frac{gm}{gd}\right)^4$	$\propto \frac{1}{gd}\left(\frac{gm}{gd}\right)^2$

Table 1 shows the comparison result between the proposed circuit and IAFCCM under various input circuit. Input current changes from 5µA to 400µA. When the input current is lower than 400µA due to the MOS transistor sizes of the proposed circuit are smaller than IAFCCM. But the output impedance R_{out} of the proposed new circuit is larger than that of the IAFCCM.

CONCLUSION

A high output impedance and high accuracy current mirror is proposed and analyzed in this paper. According to the simulation results the accuracy and the output impedance of the proposed circuit is better than IAFCCM. The proposed current mirror is much suitable for using in high linearly, high output impedance current output stages and the operational amplifiers design.

REFERENCES

1. Kuo-Hsing Cheng, Chi-Che Chen Chun-Fu Chung. Accurate current mirror with high output impedance.
2. Handkiewicz, A., Kropidlowski, M., Lukowiak, M. Switched-current technique for video compression and quantization. *ASIC/SOC Conference*. 1999; 299–303p.
3. Harb, A.; Sawan, M. New low-power low-voltage high-CMRR CMOS instrumentation amplifier. *Circuits and Systems*. 1999; 6: 97–1 00p.
4. Zeki, A., Kuntman, H. High-output-impedance CMOS dual-output OTA suitable for wide-range continuous time filtering applications. *Electronics Letters*. 1999; 35(16); 1295–1296p.
5. Nooshabadi, S., Visweswaran, G.S., Nagchoudhurhi, D. Current mode ternary D/A converter. *VLSI Design, 1998. Proceedings*. 1998; 244–248p.
6. P. E. Allen, D. R. Holberg. CMOS analog circuit design. New York: Holt, Rinehart and Winston; 1987: 233p.
7. Song, B.G., Chang, I.K., Kwon, O.J., et al. A simulation-based analog cell synthesis with improved simulation efficiency. *Tencon 99. Proceedings of the IEEE Region 10 Conference*. 1999; 2: 1018–1021p.
8. Zeki, A., Kuntman, H. Accurate and high output impedance current mirror

suitable for CMOS current output stages. *Electronics Letters*. 1997; 33(12): 1042–1043p.

9. Saclunger, E., Guggenbuhl, W. A high-swing, high-impedance MOS cascode circuit. *Solid-state Circuits, IEEE Journal*. 1990; 25(1): 289–29p.
10. B. Razavi. Principles of data conversion system design. New York: IEEE Press; 1995.