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VHDL MODELING OF PAYLOAD DATA STORAGE AND DATA PROCESSING BLOCK OF WI-FI MAC LAYER FOR TRANSMITTER.

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Abstract

For the wi-fi conversation, IEEE 802.eleven is one of the protocols to be had. The IEEE 802.11b uses the medium get right of entry to control layer (MAC) for wi-fi neighborhood region community. these wi-fi neighborhood place networks use carrier sense more than one get admission to with collision avoidance (CSMA/CS) for the MAC layer .however most effective the MAC layer for transmitter is taken into consideration here for simulation. So, the wireless transmitter module is divided into five blocks i.e. information Unit Interface block, Controller block, Pay Load data storage, MAC Header register block and records Processing block. in this paper we recollect only the simulation of MAC header sign in blocks. So, other blocks i.e. facts unit interface block, Controller block, pay load records garage block & information Processing block are not discussed similarly on this paper. A subject programmable gate array (FPGA) device has been used because the hardware implementation platform. The proposed MAC-layerhardware is carried out with Xilinx xcv300e Virtex E FPGA.

Keywords:*wi-fi MAC layer, IEEE 802.11b, Header block, FPGA, common sense analyzer*

INTRODUCTION

wi-fi verbal exchange may be very popular in contemporary lifestyles nowadays. IEEE 802.11a/b/g (ANSI/IEEE general 802.11, 1999; Stallings, 2004) WLAN collection standards provide a greater convenient surroundings to get entry to the internet for humans anywhere. An green 802.11a/b/g MAC-layer can offer suitable overall performance and throughput for some killer applications, inclusive of real-time voice communique and video conferencing. inside IEEE 802.11a/b/g standards, the MAC layer has sub-layers (Litwin, 2001). The decrease one is the distributed coordination function (DCF),

which makes use of an Ethernet-fashion rivalry set of rules that substances get right of entry to to all traffic. widespread asynchronous visitors uses this coordination characteristic. The top MAC sub-layer is the point coordination characteristic (PCF) i.e. a centralized MAC algorithm that elements competition-free provider with the aid of polling cell devices in flip. better-precedence visitors uses the PCF characteristic for information exchanges. The bodily layer (PHY) defines the frequency band, the facts charge, and other details of the real radio transmission [1].

With the growing call for & penetration of wireless services, customers of wireless network now expert nice of carrier & performance similar to what is to be had from constant networks. Media get admission to control (MAC) protocol in wi-fi community controls & the get entry to & packet transmission thru the shared channel in a dispensed manner, with minimal possible overhead concerned [2]. A MAC protocol need to offer an green use of the to be had bandwidth. The 802.11 MAC works with a single first-in-first-out (FIFO) transmission

queue. in advance [3], we've got offered the paper on VHDL modeling of payload facts storage and statistics processing block of wi-fi MAC layer for transmitter. The shape of the prevailing paper is as follows: In segment 2 we introduce the MAC body format, in section3, we gift wi-fi features, phase 4 describes the proposed block diagram of the transmitter. segment 5 describes one of a kind modules of MAC header sign in block and their function.

phase 6 describes one-of-a-kind deal with discipline registers and phase 7 describes VHDL modeling of MAC layer for the transmitter. phase eight describes simulation, experimental consequences and discussion.

MAC FRAME FORMATS

The casing starts with a MAC header .The begin of the header is the body oversee train then a field that incorporates the length realities for the system portion vector saw by method for the three tending to fields. the accompanying subject incorporates outline arrangement measurements. The last field of the MAC header is the fourth adapt to subject. Taking after the MAC header is the edge body. The last field inside the MAC body is the body investigate arrangement. every casing incorporates the accompanying basics parts,

MAC header: carries frame manipulate, duration identification, deal with (1-four) & series control facts.

frame body: contains records specific to the body kind in variable length (zero-2312 bytes).

frame check collection (FCS): IEEE 32 bit cyclic redundancy take a look at (CRC) consists of end result of making use of CRC-

32 polynomial to MAC header & body body.

The MAC frame layout comprises of a set of fields that occur in a set order in all frames [4] [5].

WIRELESS FUNCTIONS

wirelesswi-fi constancy [802.11 family of standards] is the wireless manner to address networking. it's also recognized as 802.11 networking and wireless networking. the biggest gain of wireless is its simplicity .however, wireless networks cannot provide the equal safety on the bodily level that wired networks offer. Bluetooth and IEEE 802.eleven(wi-fi) are two communique protocol requirements that outline a bodily layer and a MAC layer for wi-fi communications within a short variety (from a few meters up to a hundred m) with low power consumption .Bluetooth is oriented to connecting close devices, serving as an alternative for cables, while wi-fi is orientated closer to laptop-to-pc connections, as an extension of or substitution for cabled LANs [6].

PROPOSED BLOCK DIAGRAM OF TRANSMITTER

As discussed in advance, the transmitter block is divided in to 5 components as shown in fig (1) and handiest one block is considered for VHDL simulation. in this paper, we recollect handiest the simulation of MAC header sign up block. So, different blocks i.e. information unit interface block, Controller block, pay load records garage block & records Processing block are not discussed further in this paper.

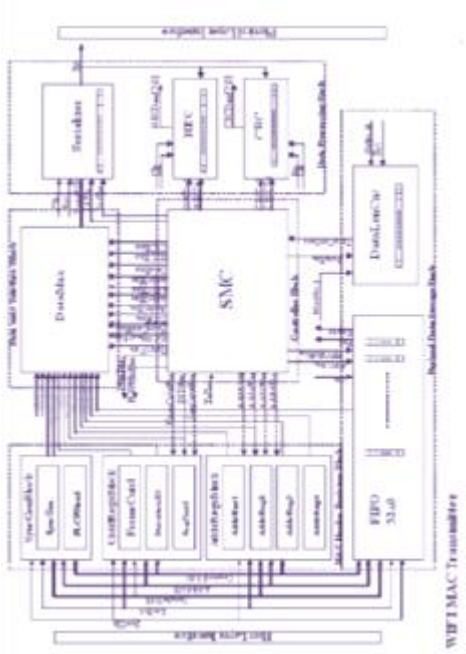

Fig 1. *Block diagram of transmitter*

One Of A Kind Modules Of MAC Header Register Block

Synchronous Generator Module

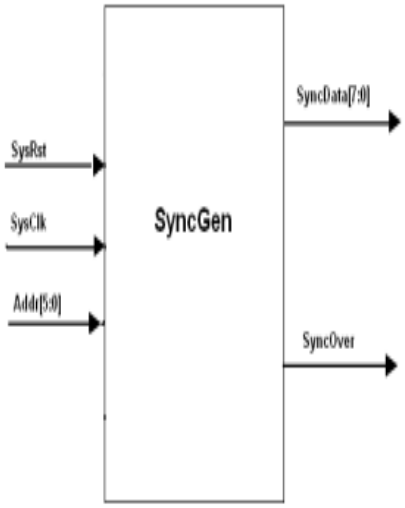

Fig 2. *Synchronous Generator Module*

It generates "Synch bit" & "SFD bit". Synch Bit is an 80 bit sequence of alternating zeros & ones, that is usedby way of the PHY circuitry it select the correct antenna & to reach constant nation frequency offset correction & synchronization with the received packet timing. SFD is the start frame Delimiter which includes the 16-bit binary sample 0C & BD which is used to outline the frame timing. At very rising edge of the Sysclk it generates the required SyncData. After the generation of the required bit the SyscOver bit is generated.

Header: The p.c. Header is always transmitted at 1Mbit/s

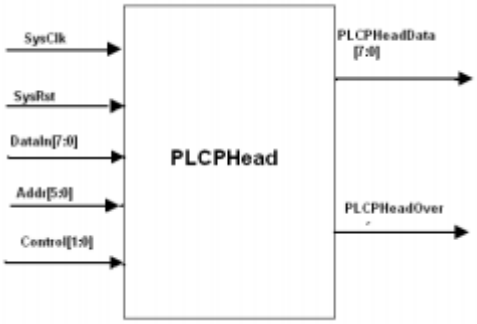

Fig 3.*PLCPHeader Module*

It carries the Logical data so that it will be utilized by the PHY Layer to decode the frame & it consists of:

1. PLCP_PDU length phrase-this represents the number of bytes contained in the packet, this is beneficial for the PHY to correctly discover the stop of packet.
2. percent Signalling subject-This currently carries handiest the price information, encoded in zero.5 Mbps increments from 1Mbps to four.5Mbps.
3. Header errors check subject-that is a sixteen bit CRC errors detection field [6].At each rising edge of the SysClk while the percent Header is enabled the specified p.c. HeadData is generated. After this generation the % HeadOver is generated indicating the give up of the p.c. Head era [7].

5.3. Frames & frame Controller

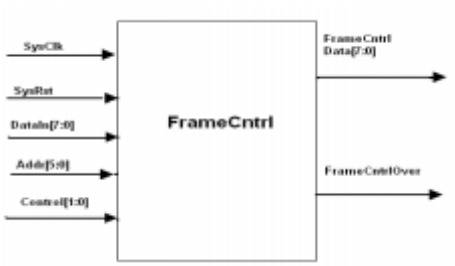

Fig 4.*Frame Control Module.*

There are 3 primary types of frames as proven beneath,

1. data frame: used for data transmission.

2. manage body: which might be used to control get admission to to the medium (e.g. RTS,CTS, & ACK).

3. management body: which are frames which might be transmitted the same way as records frames to trade

control records, but are not forwarded to higher layers [7].

body formats: All 802.11 frames are composed with the aid of the following components.

5.4- id:

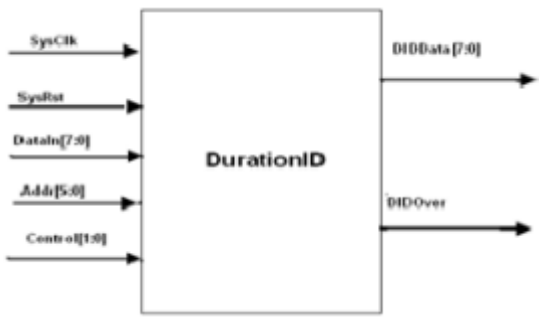

Fig 5.*duration/identity Module.*

This generates the bits which has that means depending on the frame kind. In electricity keep ballot message that isthe station identification, & in all different frames that is the period cost used for the NAV calculation [7]. At each rising fringe of the SysClk& when the period identification is enabled the required sixteen-bits is generated. After

a success era of the bits the DIDOver bit is generated.

SEQUENCE MANAGE

It includes the facts of the collection quantity of the statistics so that the proper ordering of the records takes region

on the receiver. Ti works at the growing fringe of the clock while the sequence allow sign is high.

The simulation effects of the DurationID& the series control is same because the body manipulate module.

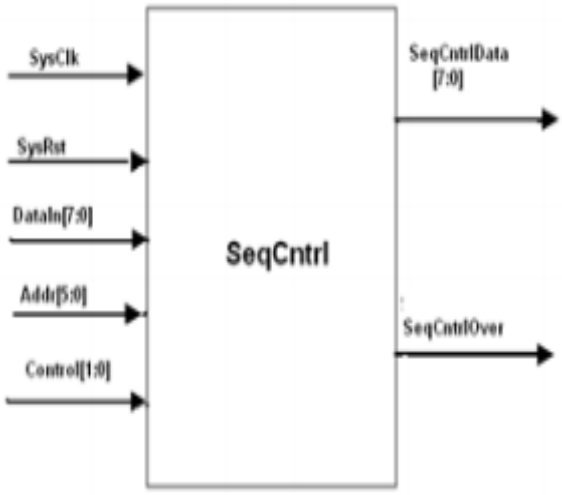

Fig 6.*series control Module.*

COPE WITH FIELDS

A body might also incorporate up to4 address depending at the ToDS&FromDS bits described within the manage fields. They are:

Deal With Register 1

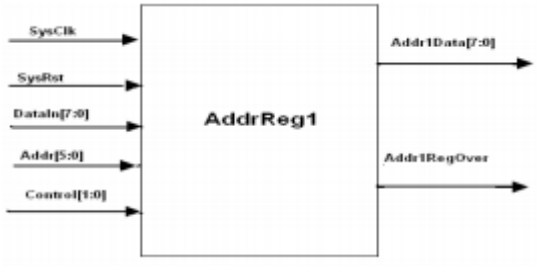

Fig 7.*Cope With Register1 Module.*

Out of four 16-bits cope with register that is first sign up named as AddrReg1. It includes the recipient address (i.e.
the station at the BSS who's the instant recipient of the packet), if ToDS is about this is the deal with of the
AP, if ToDS isn't set then this is the deal with of the stop-station [7].

Cope With Check In 2

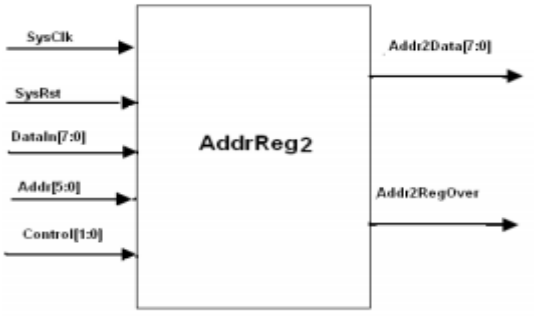

Fig 8.*deal with Register2 Module*

It includes the transmitting deal with i.e. the station this is physically transmitting the packet. If from DS is set
that is the cope with of the AP, if it isn't then it is the address of the station [7].

SIMULATIONS, EFFECTS & DISCUSSION

The MAC Header check in block consists of a complete of 6 exclusive person modules i.e., Synchronous generator,
% Header, Frames and frame controller, duration identity, series control and cope with sign in modulesrespectively .these kinds of modules are simulated the use of modelsim and simulation results are shown in Fig (eleven), Fig

(12), Fig(thirteen) and Fig(14).note that, the simulation effects of the length identity and the collection control are equal because the frame control module.

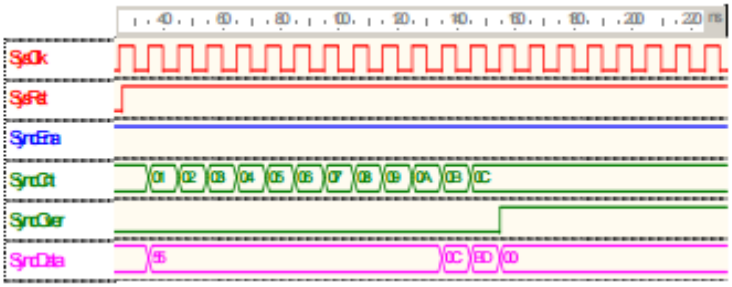

Fig 9: *Simulation of synchronous generator*

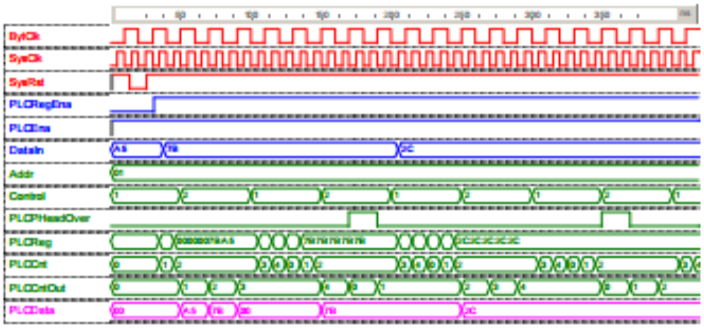

Fig 10 *Simulation of % Header*

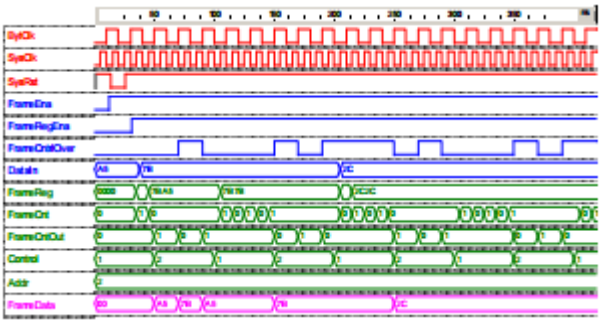

Fig 11: *Simulation of frame manage module*

For, Verification of system architecture by way of hardware, after simulation of the one-of-a-kind MAC layer blocks, the packages had been downloaded to FPGA board to confirm MAC function. The whole block was down loaded on xcv 300e vertex E improvement board. Then used good judgment analyzer to verify the consequences obtained from the simulation above.

CONCLUSIONS

we have implemented the transmitter of IEEE 802.eleven MAC layer capabilities in FPGA. The structure of thisproposed module consists of five specific modules

inside the circuit however simplest simulation of MAC header block is considered right here. various man or woman modules of MAC Header transmitter block had been designed, established functionally the usage of VHDL-simulator, synthesized with the aid of the synthesis device and a final net list has been created. end result acquired from simulation indicates that MAC header sign in block is implemented effectively & the transmitter is able to transmitting the frame formats in keeping with 802.eleven specs.

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