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High Performance Pre-computation based Self-Controlled Precharge-Free Content-Addressable Memory

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Abstract

Content-addressable memory (CAM) is a special type of memory used in networking applications for very-high-speed searching operation. It compares input search data with the table of stored data, and returns the address of matching data in a parallel search method. Also the use of parallel comparison results in reduced search time, it also significantly increases power consumption when compared to precharge based CAM. The low-power NAND-type and high-speed NOR-type CAM methods require the precharge prior to the search. This PF phase leads to increase the settling time of the output and also reduce the speed of the search operation. In this paper, a High performance Pre-computation Based Self-Controlled Precharge-Free CAM (PB-SCPF CAM) structure is proposed for high-speed applications which reduce the settling time as well as improve the speed of the search. Where search time is very important for designing larger word lengths, SCPF architecture is efficacious in applications. The experimental results show that PB-SCPF approach can attain on average 32% in power reduction and 80% in delay reduction. The most important contribution of this project is that it offers theoretical and practical proofs to verify that our suggested PB-SCPF CAM system can achieve greater power reduction without the requirement of special CAM cell design. This shows that the approach which we have used is more flexible and adaptive for general designs and high speed applications.

Index Terms – *Content-Addressable Memory (CAM), ML delay, high speed search, Self-Controlled Precharge-Free CAM.*

INTRODUCTION

The present and future Internet usage mainly depends on performance and security issues. Content-addressable memory (CAM) is useful for high-speed search operation which performs the search in a single clock cycle [2], [3]. In a CAM, the content which is to be searched is provided by user, and the CAM responds back the address location or performs association. Various routing applications and hardwares such as cache memories, network router, longest prefix matching, and radix trees use CAMs [4]–[6]. Hence, many of the table lookup tasks at different network layers that were initially implemented in software are substituted by hardware solutions such as CAMs to meet the performance requirements.CAM stores the data in its memory through bit line drivers. The input data driver feeds the search content to CAM, which performs the search operation. Next, the search line drivers gives the search word onto the differential search lines, and each CAM core cell compares its stored bit against the bit on its corresponding search lines. Match line delays on which all bits match remain in the precharged-high state. MLs that have at least one bit that misses, discharge to ground. The MLSA then detects whether its ML has a matching condition or miss condition. Finally, the encoder maps the ML of the matching location to its encoded address. The key challenges for CAM designers were to implement high-performance, low-power cells to meet the lower technology node requirements. Fig. 1 shows the conventional CAM

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organization, which performs the search operation, where the information is stored in rows and a parallel search is performed [6], [7]. CAM stores the data in its memory through the bitline drivers. The input data driver feeds the search content to CAM, which performs the search operation. It produces the match address, if any stored data matches with the search content [7].

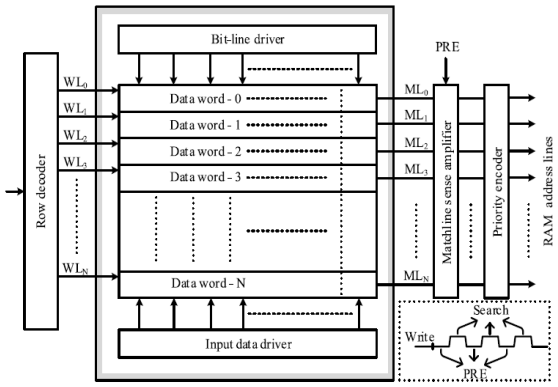

***Fig.1** Organization of a CAM Array and its Sensing Structure*

To retrieve the match information a sense amplifier is used. Each search operation is done by a precharge phase, a constraint to the faster search frequency. It is a great challenge to design a high-speed CAM for larger word lengths. Recently precharge-free CAM (PF-CAM) architectures have been given [12]–[14], but these lack the search performance at higher word lengths. To avoid the reliance among CAM cells a self- controlled PF-CAM (SCPF-CAM) has been reported in this brief which also improves the frequency of operation.

The remainder of this brief is organized as follows: Section II illustrates the conventional NAND-type CAM operation. Section II illustrates the conventional NOR-type CAM operation. PF-CAMs are illustrates in Section IV, where the proposed PB-SCPFCAM has been introduced. In Section V, the performance comparison results derived from the post layout simulations carried out on the compared designs of a 128 × 32-bit CAM array have been presented and Section VI concludes this brief.

NAND-TYPE CAM

NAND-type CAM cell is used to lessen the power consumption of the system. In a conventional CAM, before carrying out a search, all match- lines (MLs) should be precharged. Due to the consumes of more power it will reduces the performance and frequency of operation because of the need of an extra precharge phase. A pre-computation stage is proposed to remove unwanted frequent charging and discharging of all ML nodes. In differential ML with a self-disabling sensing technique has been used to choke down the ML draining current. Employing differential ML instead of a single-ended ML helped boost the search speed without the overhead of power consumption. A search is performed in a CAM through three phases: data write, precharge, and data search. A NAND-type ML CAM cell, consists of one SRAM cell and a pair of nMOS transistors in the comparison circuit and one nMOS transistor (M9) in evaluation logic is depicted in figure. The bitline pair (BL, BL) is used to store the data in the CAM cell and search-line pair (SL, SL) has been used to find the content in CAM cell.

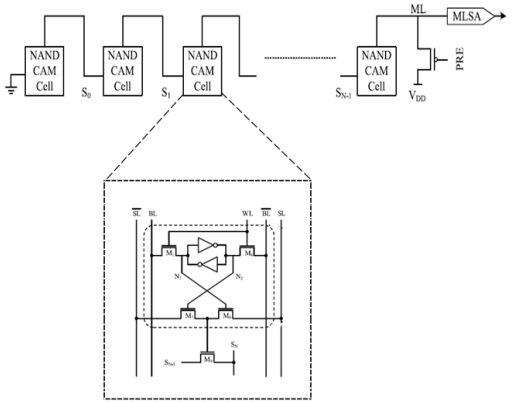

***Fig. 2** Word Structure of NAND-Type CAM*

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Before performing each search, all Match Lines must be precharged to the supply voltage by keeping search-lines at low. If the provided search content is matched with the stored data, ML discharges to a low value (GND); Otherwise Match Line value remains at a precharged value. Before each search, the ML has to be precharged; hence, NAND-type ML is not favored for CAMs with long words due to the larger delay.Moreover, it suffers from the charge-sharing problem across the PASS transistors. Because of this drawback NAND-type ML is ideal only for CAM with a small word length.

Limitations of NAND-type CAM: Prior to any search operation ML (ML) has to be precharged. The speed of the search operation is constrained by the precharge cycle. Speed of the search was lessened because of its larger delay. It suffers from the charge-sharing problem across the pass transistors. NAND-type ML is preferred only for CAM with a small word length.

NOR-TYPE CAM

To make the system's performance more better, NOR-type CAM cell is used. Moreover, the speed of the search operation is enhanced when compared to the NAND-type CAM. Conventional NOR CAM cell consists of two parts. First part is used for storing the data, which is known as store unit and the other part is used for comparing data, known as compare unit. The store unit is usually implemented as the traditional 8T SRAM cell, which has a cross coupled inverter pair. The compare unit is a pass-transistor logic (PTL) which is used for comparing the stored data with the search data.

The CAM cell in NOR-type CAM design is XOR-type. Moreover, pull-down transistors of each CAM cell are arranged in NOR type. Each search operation consists of two phases: Precharge phase and Evaluation phase. In the precharge phase, PRE = 1 will precharge the ML to high. After that, PRE is dragged down to 0 to initiate the evaluation phase. If there is any mismatch the ML is discharged to 0 instantly as the pull-down path is very short. Threfore we can say, the NOR-type CAM gives the best search performance.

For example, in the CAM tag used in the translation look-aside buffer or cache memory, at most one word is matched on each lookup, which means that almost all the MLs would be discharged to 0, and then be charged to high before the next search. NOR-type CAM can provide the best performance.

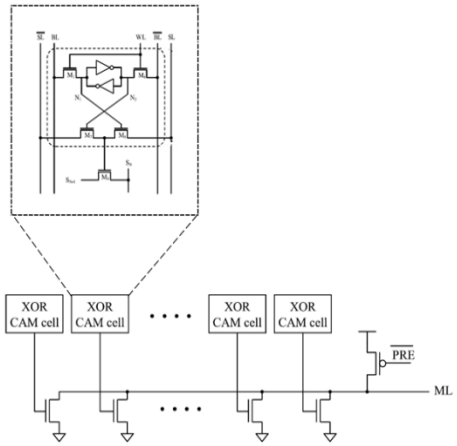

Fig. 3 *Word Structure of NOR-Type CAM*

the NAND-type CAM in comparison to the NOR-type CAM, targets to lessen the power dissipated in search operation, where the pull-down transistors of each CAM cell in the same word are arranged in NOR type. At first, the ML is precharged to 1 and discharged to 0 only when all CAM cells are matched. The power consumption is minimal as the load capacitance of ML is minute and very less MLs are discharged to 0 during the search. In case of a match the ML discharge is very slow as the pull-down path is very long.

Limitations of NOR-type CAM: NOR-type ML feels SC current in the precharge phase. NOR-type CAM is power

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inefficient. It gives bad performance for a large power saving. Moreover, before each search ML (ML) has to be precharged.

PRECHARGE-FREE ML STRUCTURE

Precharge-Free CAM

The main puropose of PF CAM was to perform the search operation for larger word lengths which could not be achieved by conventional type CAMs. Moreover, by eliminating the PRECHARGE phase speed of the operation is improved. The development of a CAM structure is carried out with a PRE signal, which ends up at a lower speed of search operation. This problem has been eradicated by eliminating PRE phase, as described in Figure 3.3. Instead, they used control bits (CBs), because of which the overall search time is reduced by one level. In a CAM, the first operation is write, the next one is precharge, and then search. Whereas the write is followed directly by the search phases in the PF-CAM architecture. The operation of the PF-CAM is as follows:1) While storing the data, CB is set to a high value (logic 1). This setting of CB turns M0 OFF and, simultaneously, M1 ,……MN−1 will be turned OFF as T0 ,T1,……TN−1 are ON, which will provide GND directly to the gate of M1 ……MN−1, as shown in Figure 3. 2) Once the data are stored, CB is reset (0) and this will turn ON M0 as M0 is a pMOS, since the source of M0 is connected as a control to M1 , thus S0 value is passed to the gate of M1 , which is an nMOS. If CAM cell-1 is matched, M0 will pass logic high to M1, which will result in turning ON of M1. If CAM cell-2 is also matched, then in a similar fashion logic high will be passed to M3 from CAM cell-2, and likewise a cascaded chain of CBs will be passed from one cell to another. If there is a mismatch at any cell, then the upcoming cells will be turned OFF. Hence, there is an advantage of PF-CAM structure as it reduces the number of SC paths, which results in overall reduction of power usage. Because of the cascading of CAM cells overall, the speed of search operation is notably reduced.

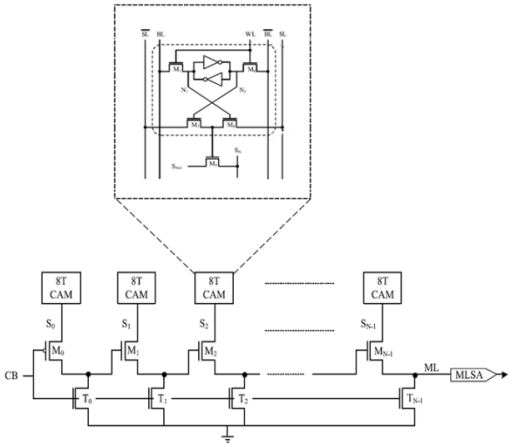

Fig. 4 *Word Structure of PF CAM*

B. Self-Controlled Precharge-Free CAM

SCPF-CAM structure, resolves the imperfection of all the mentioned problems which are present in the precharge-based CAMs. Moreover, it enhances the speed of operation when compared to the PF-CAM architecture. An 8T CAM cell has been used as the basic block to design a word. There are two key contributions which are done, they are:

1) Self-control operation, where the charge stored at the node S controls the ML transistors, thereby avoiding the dependence on previous ML value.

2) To give better search frequency, it removes the precharge phase.

The suggested PB-SCPF CAM is self-controlled; the node (S) value of the 8T CAM cell controls the evaluation logic and gives the output. It passes a high value through the transistor (NMOS) when the the prestored data is matched with the search content. Otherwise it passes a low value through the transistor (PMOS) to the ML. From the word architecture, it is well-defined that the minimum operating voltage is restricted to VTHP +2VTHN +VM. The voltage VM is the most

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dominating among the three voltages and is mostly MLSA dependent.

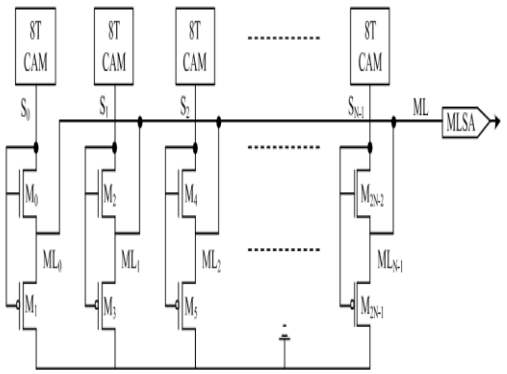

Fig. 5 *Word Structure of SCPF-CAM*

Transistor (NMOS) is selected to have a low threshold to push the supply voltage to the scaling limit. A complete comparison has been done with the NAND-CAM and PF-CAM to validate the efficiency of SCPF-CAM. The compared designs are analyzed at temperature variation and supply voltage scaling. Process variation is carried out explicitly to provide a better understanding of the device property and the application aspects of CAM.The minimum amount of time required in the conventional CAM operation is,Ttotal = Twrite + Tprecharge+ Tsearch. However, in the proposed design the minimum requirement is,Ttotal = Twrite + Tsearch.

C. Pre-computation Based Self-Controlled Precharge-Free CAM

The gain of the SCPF-CAM structure is exploited in a PB-SCPF CAM. The drawbacks of the precharge-based earlier reported circuits (which was cascading) are also taken care of by removing dependence among different CAM cells. The main benefit of this proposed architecture is that the design of larger word lengths with higher performance at a higher frequency of operation. Owing to the larger delay metric in PF-CAM, it is not beneficial for creating longer word lengths .Moreover, it can not be operated at a higher frequency of operation.

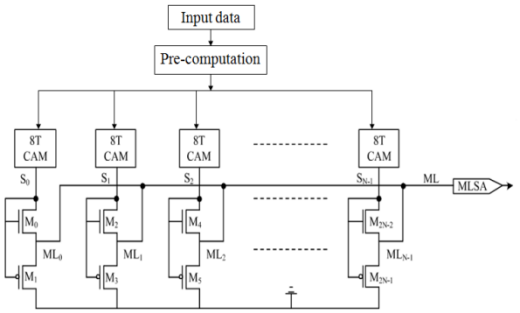

Fig. 6 *Block Diagram of PB-SCPF CAM*

In the Pre-computation Block, as a parameter for comparison operations, parity bit is used. The parity bit generator is used for generating parity bit value. When parity is used as a parameter the benefit is that when compared to the existing systems parameter memory is highly reduced as only one bit i.e. k=1 is needed to store parameter corresponding to each stored word where length of input data bits is of no significance. In pre-computation, the number of comparison operations is very much reduced causing power consumption of parameter memory to be reduced. Therefore, the overall power consumption of the CAM is reduced.

In terms of complexity and area, the proposed architecture has improvement over existing methods. As the complexity and parameter comparison operations is reduced the searching speed is also enhanced. The delay for each search operation is lessened because of the use of parity bits. Therefore, it enhances the search speed of parallel CAM. The number of bits having logic value ‘1’ in a given binary data is counted. If number of bits in the binary data is odd, then the parity bit value is ‘1’ and if the number of one’s in a binary data is even, then the parity bit value is ‘0’. The example of this process is shown in fig. 7.

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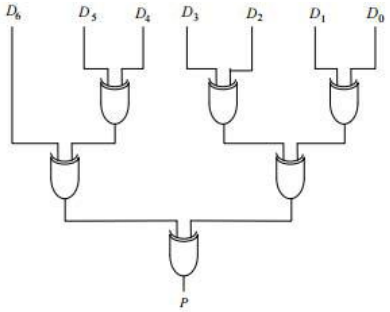

Fig. 7 *Logic Circuit of Parity Bit Parameter Extractor*

Initially, the parity bit generator extracts parity bit and comparisons of extracted parity bit are made with that of stored parity bits. As a consequence of parity bit comparisons, there is a comparison in data memory which takes place. when the corresponding parity bit is matched with the input word's parity bit comparisons in data memory of stored data words is performed.

RESULT AND PERFORMANCE ANALYSIS

A. Design process

Complete line of software solutions is given by Tanner EDA which catalyze innovation for the design, layout and verification of analog and mixed-signal integrated circuits. Customers are making breakthrough applications in areas such as, displays and imaging, power management automotive, consumer electronics, life sciences, and Radio Frequency (RF) devices.

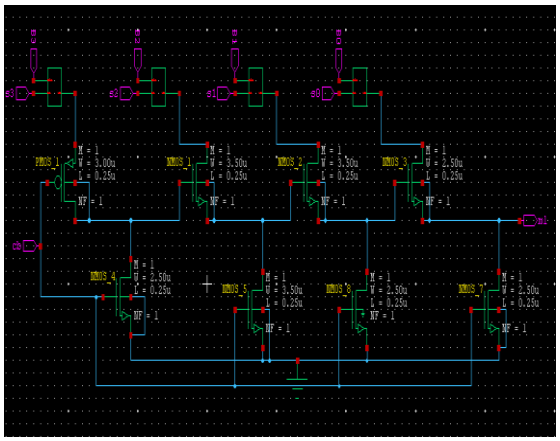

Fig. 8 *Design of PF CAM*

The schematic diagram of single PF CAM design is shown in the Fig. 8. From this design, 4*4 PF CAM was designed, as shown in fig. 9. It draws in tanner EDA tool S-Edit window. Then it runs by using T-spice. The output waveform which is illustrated in fig. 10 and their power analysis was performed. The total power consumption is 0.00139 mW.

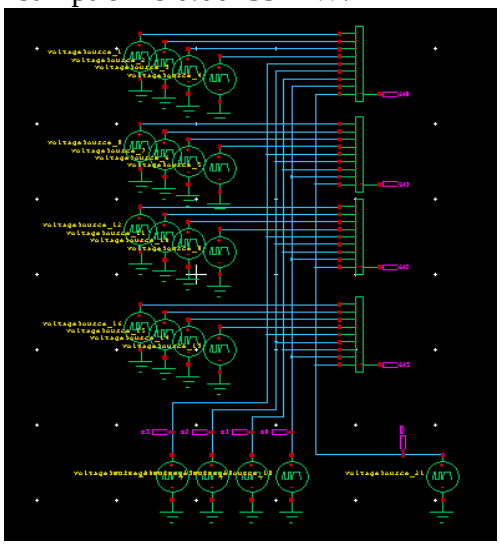

Fig. 9 *Design of 4*4 PF CAM*

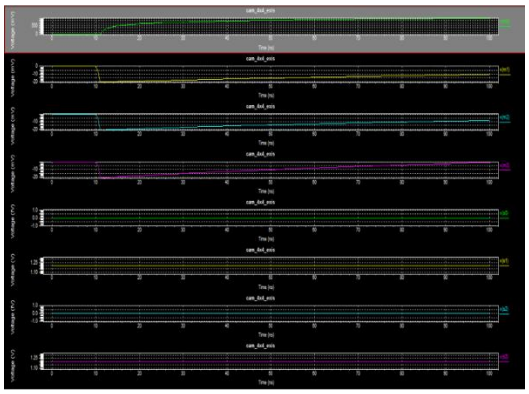

Fig. 10 *Output Waveform of PF-CAM*

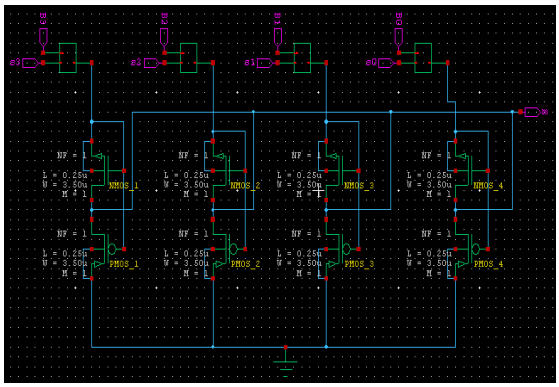

Fig. 11 *Design of SCPF CAM*

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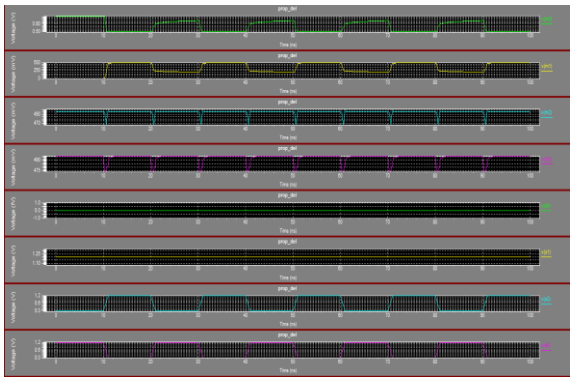

Fig. 12 *Output Waveform of SCPF CAM*

In the Fig. 11 the schematic diagram of single SCPF CAM design is shown. From this design, 4*4 SCPF CAM was designed. It draws in tanner EDA tool S-Edit window. Then it runs by using T-spice. The output waveform given in fig. 12 and the power analysis was performed. The total power consumption is 0.1338 mW.

B. ML Delay Analysis

The most important performance parameter in CAM design is Match Line delay, and to measure the frequency of operation and its applicative aspects calculation and analysis are required. A thorough study of ML delay was performed on compared designs with the earlier method outcomes. Moreover, its dependency on various parameters for example temperature and voltage has been accorded. As there is increment in the temperature, gradual decrement in the delay metric is observed ; the related observations for this is shown in Fig. 5(a). Because of the access time when the supply voltage is increased, the delay also increases. The gate switching takes a longer time, as more charge has to be moved in an entire row and line delay is increased, as every wire has a capacitance. While increasing temperature, false match occurs in case of all the mismatched MLs in NAND-CAM. At above 40 °C temperature, as there is decrement in threshold drop with the increment in temperature the design does not work. While increasing the temperature there is a probability of wrong state increases.

C. Process Variation Comparison

Process variation analysis is done at different corners (FF, FS: Fast; SS, SF: Slow; TT: Typical) on the proposed and compared CAMs. The NAND-type ML CAM does not work at the extreme corners (FF and SS) after half the search time period; the mismatched ML values tend to match during the end of the search phase, which results in a wrong address output. For larger word length designs, the voltage at the final stage is less and also unable to drive the forthcoming cells due to the dependence between CAM cells. The PB-SCPF CAM works well at all these corners and the compared results will be good.

D. Search Delay Reduction by Proposed SCPF-CAM

Because of the capability of the suggested design to operate without a PRE phase, there was a noteworthy lessening in the delay (considering the PRE time), which provides the suggested design to work at a higher search frequency with respect to the compared designs. We attained a 73% and 88% reduction in delay compared to NAND-CAM and PF-CAM, respectively, at 27 °C and VDD of 1 V. , More search operations can be performed because of this advantage in the ML delay reduction, which in turn causes a decrement in the required number of search bits. This permits the design of larger word structures with higher performance; the correlated results are shown in Fig. 5(b).

E. Performance Comparison Summary

The performance summary of the compared designs is summarized in Table III. The SCPF-CAM gives ML value in the least time among the compared designs at the cost of minuscule additional dissipation. An increase in peak power is seen in all the compared designs with the increment in supply voltage. In Fig. 5(c)

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the peak power comparison at different temperatures is shown. A noteworthy growth in peak power is seen in PF-CAM. Hence, in our suggested design, the particular increment is very small. In comparison to other designs, the suggested PB SCPF-CAM uses reduced peak power. The NAND-type and PF-CAM are sensitive to the data pattern and process corner. At low supply voltage and high ML-size, the performance degrades for these designs. In Fig. 2 transistor M9 in the SCPF-CAM cell having low voltage threshold is shown, which is the cause for additional energy dissipation. The importance of it is described through the worst case scenario of the 1-bit mismatch summarized in Table IV at various search durations. The proposed design performance is reasonable at this condition, but the other designs do not function. Search operation is performed by the given scheme in a lower search durations, whereas at lower search durations the compared designs do not function. PRE phase in the proposed design is removed which is a requirement of referred designs causing one phase delay to be reduced. The ML delay is higher than in some of the compared designs, but PRE phase duration of T ns is not taken into consideration by search, which in turn increases the frequency of operation.

CONCLUSION

For the high-speed applications, the suggested PB-SCPF CAM structure is used, as it shows the least ML delay among the compared designs. The PRE phase is avoided in the suggested PB-SCPF scheme .Moreover, this sceme abolishes the dependency between CAM cells in a word due to the self-control scheme. And also, the delay occurrence is removed. Therefore, more searches within a specified time is performed. In the suggested scheme , the ML delay is 80% of PF-CAM. This shall be of interest among designers to form larger word lengths at better search speed.

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REFERENCES

[1] TelajalaVenkataMahendra, Sandeep Mishra, and AnupDandapat, “Self-Controlled High Performance Precharge-Free Content Addressable Memory”, IEEE Trans. Very Large Scale Integr. (VLSI) Syst.,

[2] Chua-Chin Wang, Chia-Hao Hsu, Chi-Chun Huang and Jun-Han Wu, “A Self-Disabled Sensing Technique for Content-Addressable Memories”, IEEE transactions on Very Large Scale Integration (VLSI) Systems-II: express briefs, vol. 57, no. 1, January 2010.

[3] Kuludip Kumar Gupta ,Er.NitinKr.Tiwari, Dr. R.K Sarin, “NAND-NOR type 4T Loadless SRAM Based Area And Power Efficient Hybrid CAM”, International Journal Of Electronics And Communication Engineering & Technology (IJECET).

[4] Lin C.S, Chang J.C and Liu B.D, “A low-power pre-computation based fully parallel content-addressable memory”, IEEE J. Solid-State Circuits, vol. 38, no. 4, pp. 654–662, Apr. 2003.

Page 1-9 © MAT Journals 2017. All Rights Reserved

[5] Pagiamtzis.K and Sheikholeslami.A, "Content-addressable memory (CAM) circuits and architectures: A tutorial and survey," IEEE J. Solid-State Circuits, vol. 41, no. 3, pp. 712–727, Mar. 2006.

[6] Satendra Kumar Maurya and Lawrence T. Clark, Senior Member, IEEE, "A Dynamic Longest Prefix Matching Content Addressable Memory for IP Routing", IEEE transactions on Very Large Scale Integration (VLSI) Systems, vol. 19, no. 6, june 2011.

[7] Shanq-Jang Ruan, Chi-Yu Wu, and Jui-Yuan Hsieh, "Low Power Design of Precomputation-Based Content-Addressable Memory", IEEE transactions on Very Large Scale Integration (VLSI) Systems, vol. 16, no. 3, march 2008.

[8] Zackriya V.M and Kittur H.M, "Precharge-free, low-power content addressable memory," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 24, no. 8, pp. 2614–2621, Aug. 2016.

[9] Z. Cai, Z. Wang, K. Zheng, and J. Cao, "A distributed TCAM coproces- sor architecture for integrated longest prefix matching, policy filtering, and content filtering," IEEE Trans. Comput., vol. 62, no. 3, pp. 417–427, Mar. 2013.

[10] S. K. Maurya and L. T. Clark, "A dynamic longest prefix matching content addressable memory for IP routing," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 6, pp. 963–972, Jun. 2011.

[11] Y.-C. Shin, R. Sridhar, V. Demjanenko, P. W. Palumbo, and S. N. Srihari, "A special-purpose content addressable memory chip for real-time image processing," IEEE J. Solid-State Circuits, vol. 27, no. 5, pp. 737–744, May 1992.

[12] V. Lines et al., "66 MHz 2.3 M ternary dynamic content addressable memory," in Proc. IEEE Int. Workshop Memory Technol., Design Test., Rec., Aug. 2000, pp. 101–105.

[13] S. Jeloka, N. B. Akesh, D. Sylvester, and D. Blaauw, "A 28 nm configurable memory (TCAM/BCAM/SRAM) using push-rule 6T bit cell enabling logic-in-memory," IEEE J. Solid-State Circuits, vol. 51, no. 4, pp. 1009–1021, Apr. 2016.

[14] S.-J. Ruan, C.-Y. Wu, and J.-Y. Hsieh, "Low power design of precomputation-based content-addressable memory," IEEE Trans. Very Large ScaleIntegr. (VLSI) Syst., vol. 16, no. 3, pp. 331–335, Mar. 2008.

[15] P.-T. Huang and W. Hwang, "A 65 nm 0.165 fJ/bit/search 256 × 144 TCAM macro design for IPv6 lookup tables," IEEE J. Solid-State Circuits, vol. 46, no. 2, pp. 507–519, Feb. 2011.

[16] N. Onizawa, S. Matsunaga, V. C. Gaudet, W. J. Gross, and T. Hanyu, "High-throughput low-energy self-timed CAM based on reordered over-lapped search mechanism," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 61, no. 3, pp. 865–876, Mar. 2014.

[17] S. Mishra and A. Dandapat, "EMDBAM: A low-power dual bit asso- ciative memory with match error and mask control," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 24, no. 6, pp. 2142–2151, Jun. 2016.

[18] S. Mishra and A. Dandapat, "Energy-efficient adaptive match-line con-troller for large-scale associative storage," IEEE Trans. Circuits Syst. II, Exp. Briefs, Jul. 2016, doi: 10.1109/TCSII.2016.2595598.

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