# Design and Evaluation of a Majority Gate Based Encoder in Quantum-dot Cellular Automata (QCA)

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***DOI:https://doi.org/10.5281/zenodo.2533577***

***Abstract***

*Quantum-dot cellular automata are the rising nanotechnology used to structure the nano scale circuits. QCA is the powerful elective technique to the CMOS innovation. In this paper,anovel effective design of encoder is proposed by the use of Majority gate and inverter.The proposed QCA encoder 4X2 and8X3 design outshines interms of cell count, area and delay. The number of cells in QCA circuits is similar to the number of transistors in CMOS circuits. The structure is made successful by diminishing QCA wire intersection and cell. The fundamental goal is to diminish the measure of the circuit and to enhance the speed of activity of QCA circuits.*

***Keywords****-QCA, Majority gate, Inverter, Decoder, Encoder, Cell count, Crossover*

## INTRODUCTION

CMOS is a silicon transistor technology for implementing VLSI devices which faces some challenging problems such as high power consumption and difficulties in feature size reduction. Scaling is another problem of CMOS. To beat constraints of CMOS innovation, QCA is an effective elective strategy. QCA accomplishes high gadget thickness with to a great degree low power utilization and high exchanging rate without utilizing transistors. QCA give around a THz handling speed.One of the major advantages of QCA is that it acts on the principle of electron polarization. An encoder is a device that converts information from one format or code to another, for the purposes of standardization, speed or compressions.In this paper we have implemented design of 4x2 and 8x3 encoder using minimum number of cells. Design is implemented and simulated using QCA Designer 2.0.3 which gives efficient output.

## QUANTUM DOT CELLULAR AUTOMATA

QCA is a transistor-less technology, which combines the advantages of quantum dot and cellular automata logic together.Basic unit of QCA is quantum spot which is minor molecule of semiconductor materials which has width of 2 - 10nm. A quantum dot is capable of trapping electrons in three dimensions. QCA acts on the principle of electron polarization as opposed to the transmission of current through devices, thus minimizes the energy consumption [1-3].

The dots are coupled by capacitors and tunnel junctions. Electrons in the cell have the ability to tunnel from one quantum dot to the next. The electrons in the cells are used to store and transmit data.

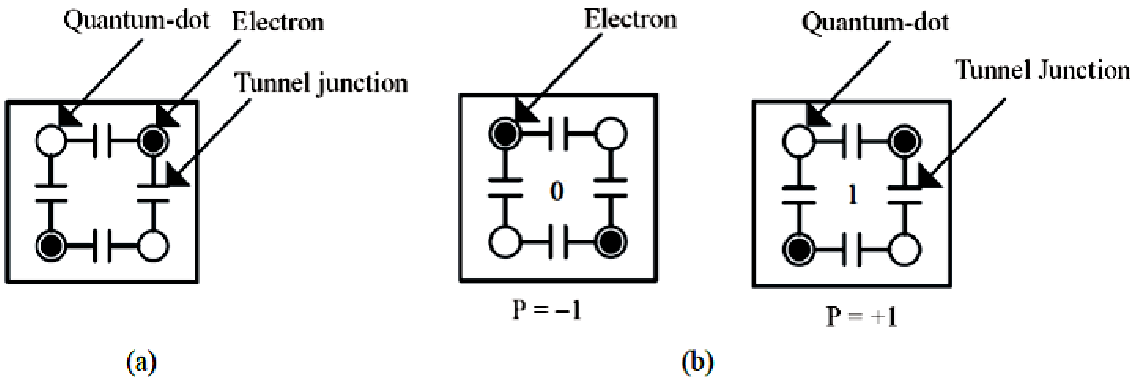
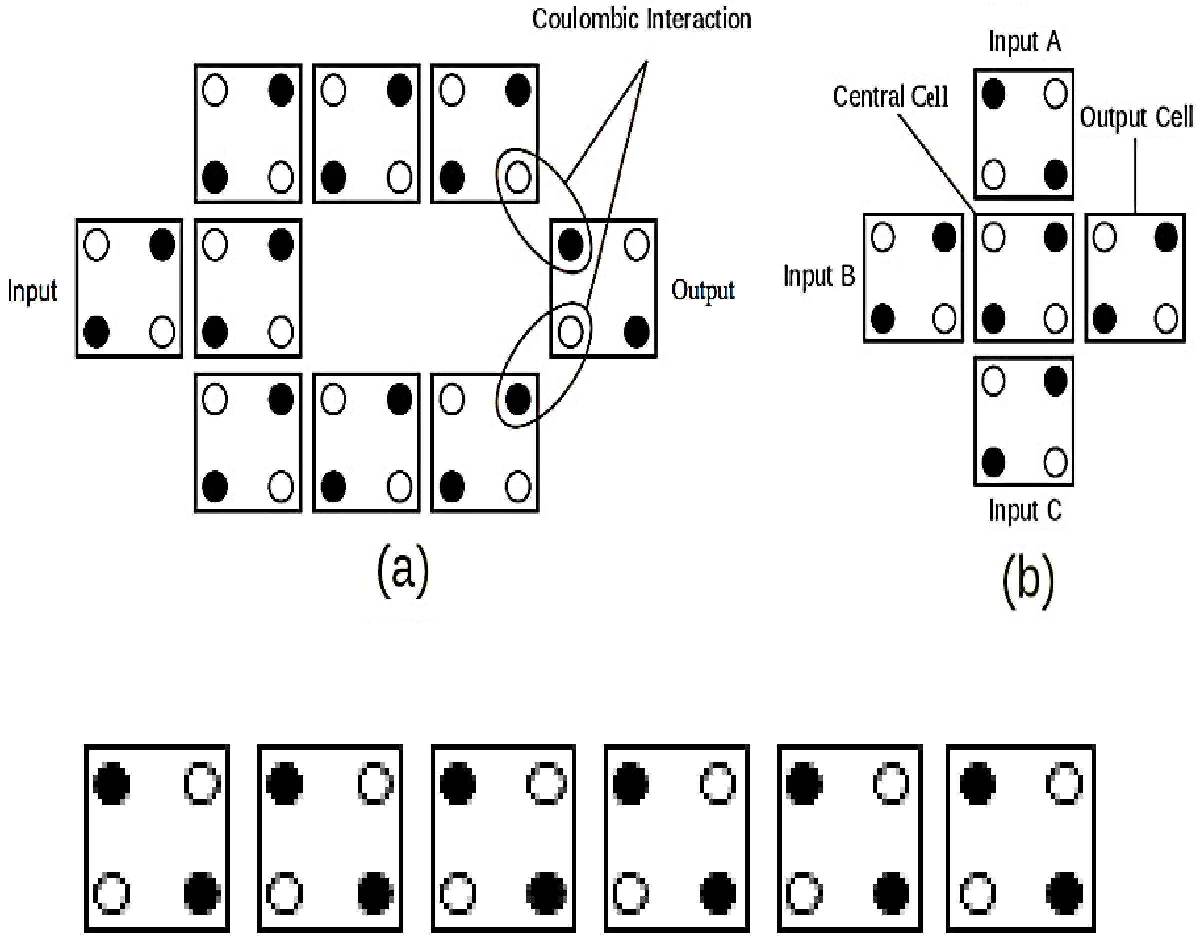



*Figure 1:(a) QCA Cell (b) QCA Cell Polarization.*

The positions of the electrons define the polarization (p) state of the cell. A binary 0 and binary 1 is represented by p= -1 and p=+1 respectively which is shown in Figure1[b]. The fundamental building blocks of QCA are inverter, majority gate and wire shown in Figure 2.




**(c) QCA Wire**

***Figure 2:*** **(***a) QCA Inverter (b) Majority Gate &(c) QCA Wire*

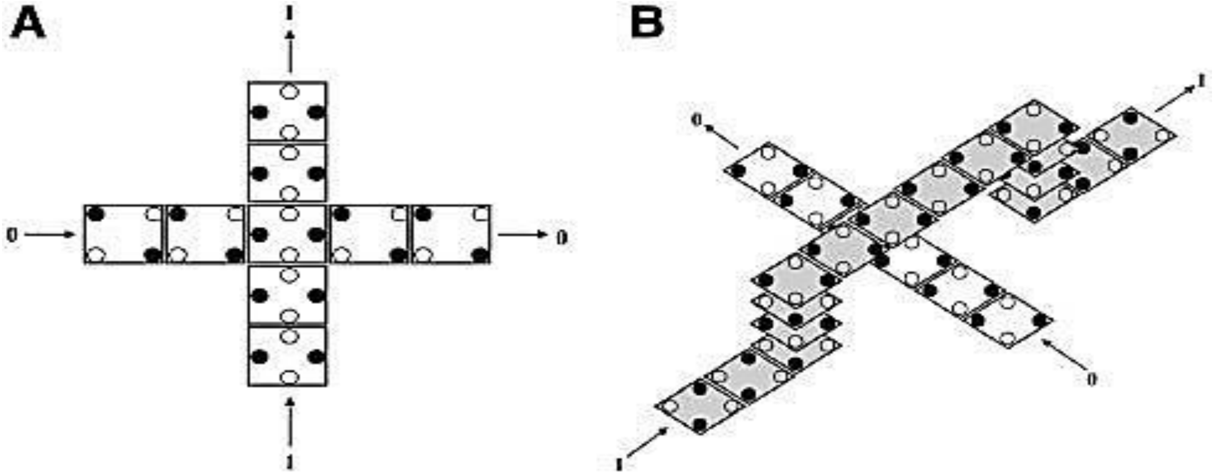



***Figure 3:****[A] Coplanar Crossing (B) Multilayer Crossing*

In QCA, the wire intersection can be performed in two different ways to be specific co-planar intersections and multi-layered intersections appeared in Figure 3.It is anticipated that the coplanar coupling is to some degree more fragile than it would have been in an ordinary wire. The stability in coplanar crossover is less compared to multilayer type crossover. But implementation of multilayer crossing in QCA is a challenging issue [4-6]. This is be-cause of the fact that QCA cells have been fabricated only in single layer. A number of variations in coplanar crossing have been proposed in order to improve its efficiency. The complexity and performanceof QCAcircuits are evaluated based on certain parameters as cell count, area, latency, the stability of output, etc.

Basic gates such as AND, OR, NOT gates can be implemented using majority gate. Using the Columbic interaction between electrons, the information can be propagated through QCA cells.

Electrostatic cooperation properties between the neighbor cells create the acknowledgment of Majority door in QCA. The output cell then reflects the information as provoked by the driver cell. Therefore, the majority function Y for three inputs A, B, C can be suggested as: M(A,B,C)=AB+BC+CA.

**QCA CLOCKING**

The clock signals are generated by an electric field which is applied to the QCA cells to change the tunneling barrier between dots. The clocks of a QCA system serve two purposes: powering the automaton and controlling data flow direction. QCA clock is used to push information from input to output by modifying cell tunneling energy. QCA clocking is made of four phase shift by 90 degree [7-8]. QCA clocking is shown in Figure 4. Four phases of clock are as follows:

**Switch phase**:The tunneling barriers between dots of QCA cell are raised. So the QCA cell becomes in polarized state.

**Hold phase**:barrier of the cell stays high and electron can't burrow among specks and the cell keeps up its present states (settled polarization).

**Release phase**: barrier between dots of QCA cell are decreased and electron can tunnel through dots. So QCA cell become in un-polarized state.

**Relax phase**:barrier stay at lowered and cell remains in un-polarized state.

Different colors mean different clock zones, beginning with green, cyan, light blue and white.

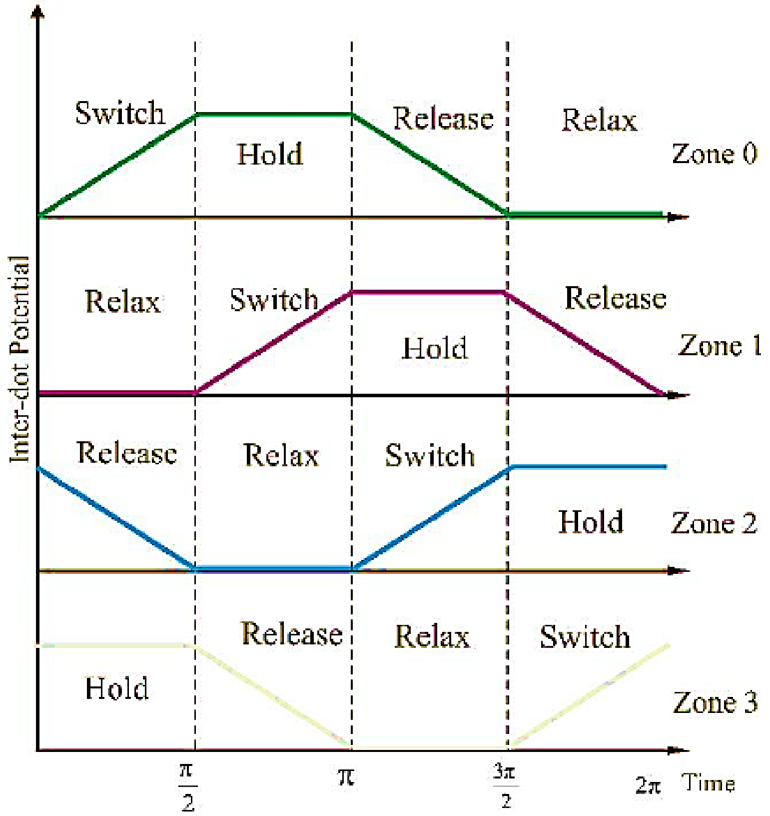


***Figure 4:****QCA Clocking*

## METHODOLOGY

The methodologies used in the proposed encoder are Quantum-dot Cellular Automata (QCA) Majority gate and Inverteris explaining in Table 1.

XOR and Decoder being two of the most useful functions in the Booleancircuit[9-11].

***Table 1:****Design Parameters for Simulation in QCA Designer*

| **Parameter** | **Value** |
|---|---|
| Cell width | 18 nm |
| Cell height | 18 nm |
| Dot diameter | 5 nm |
| Number of samples | 12,800 |
| Radius of effect | 80 nm |
| Relative permittivity | 12.9 |
| Clock high | 9.8e-22 J |
| Clock low | 3.8e-23 J |
| Clock amplitude factor | 2 |

## EXISTING SYSTEM

Decoder circuits are the existing system for this paper. A decoder is a combinational circuit that converts binary information from n input lines to a maximum of $2^n$ unique output lines in Table 2. In the existing system, decoder circuits used majority gate and conventional inverters. With QCA Designer ver.2.0.3, the circuit functionality is verified [4].Figure 5 & 6 explain the QCA design and simulation result of 2×4 encoder. Figure 7 & 8 explain the QCA design and simulation result of 3×8 encoder. Figure 9 & 10 gives the output of $D_3$,$D_7$,$D_2$,$D_1$,$D_5$ and $D_6$.

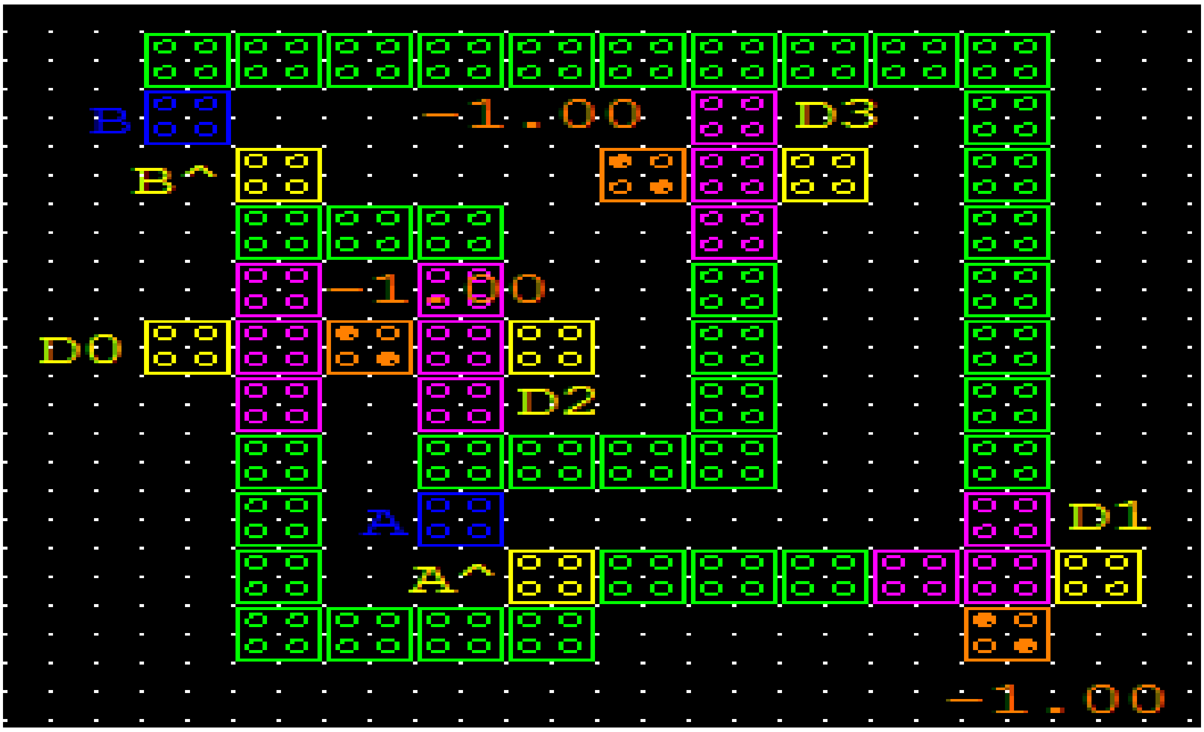



***Figure 5:****QCA Design for 2x4 Decoder*

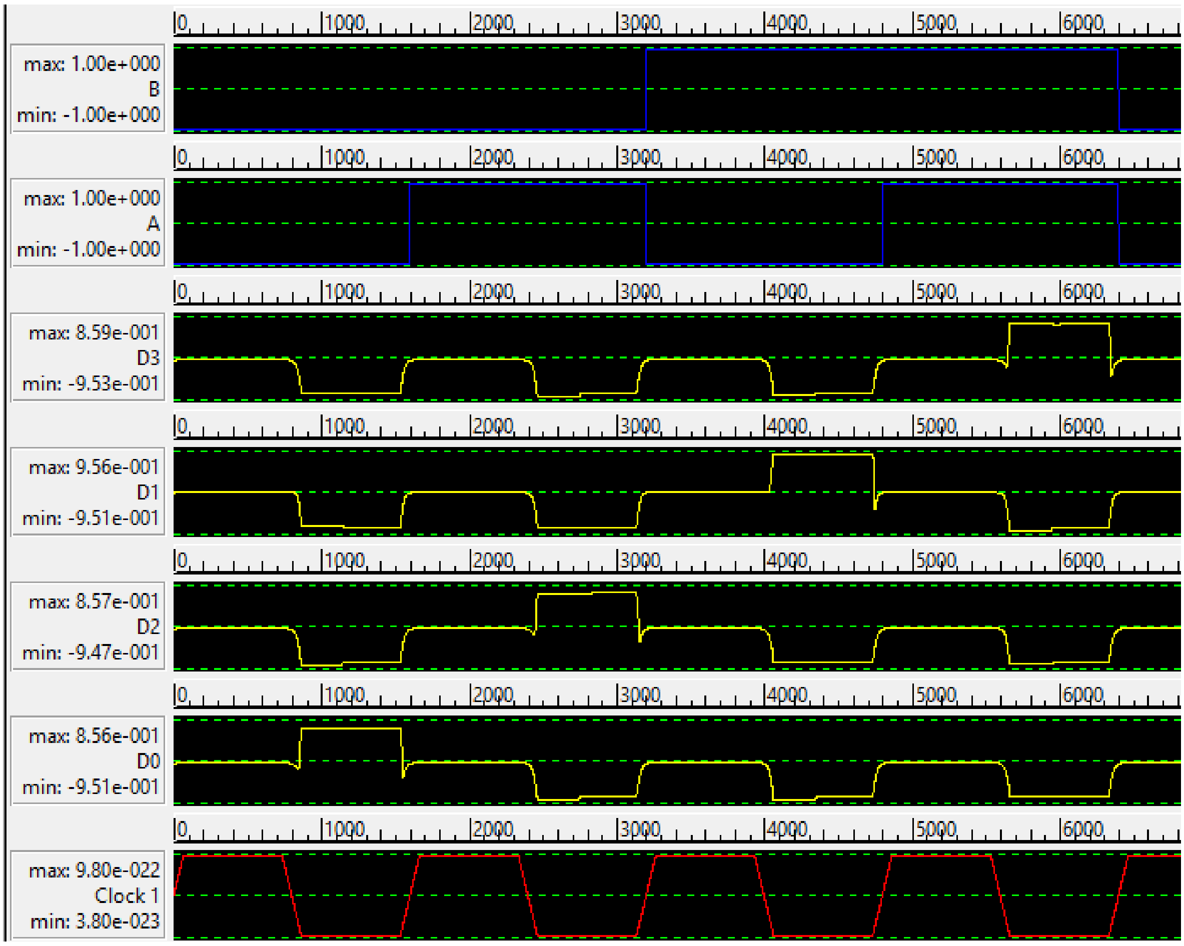



***Figure 6:****Simulation Result Of 2x4 Decoder Design.*

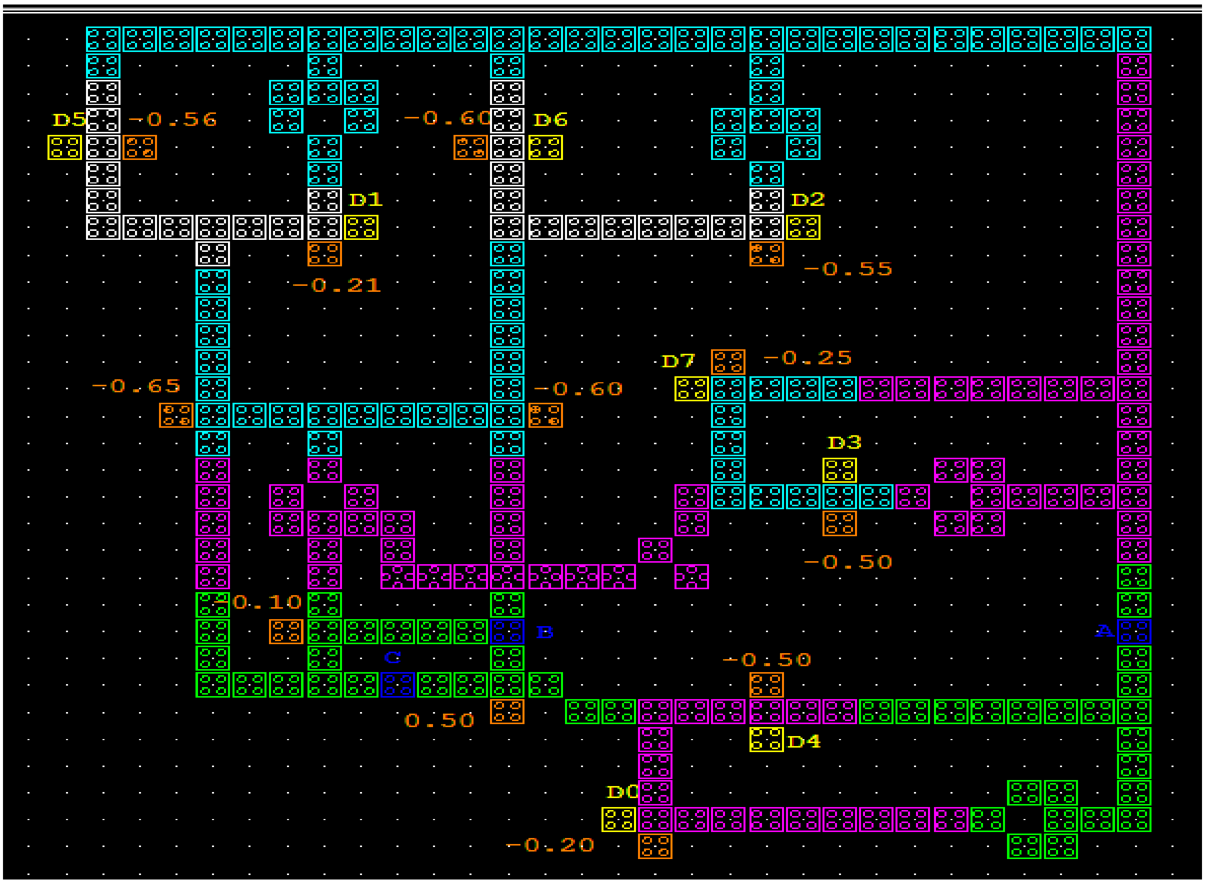



***Figure 7:****QCA Design for 3x8 Decoder*

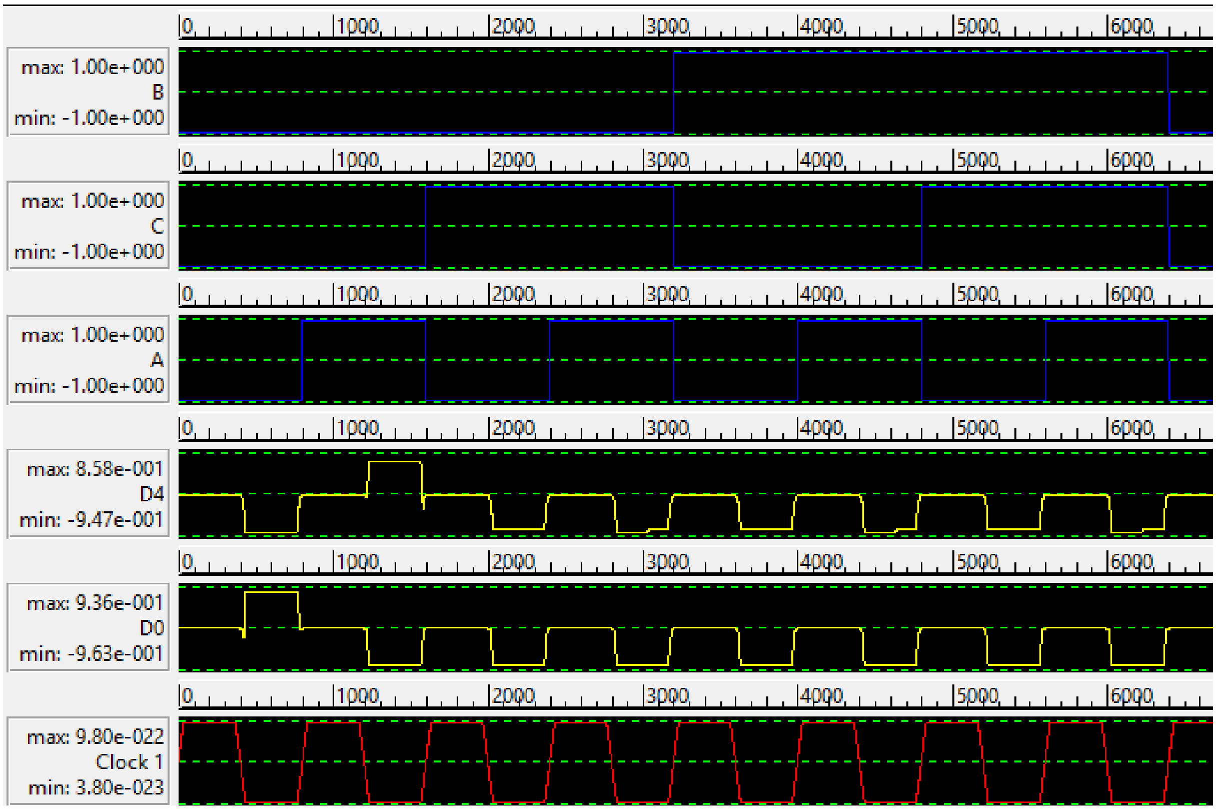



***Figure 8:****Simulation Results of 3x8 Decoder (A)Output of D0 and D4.*

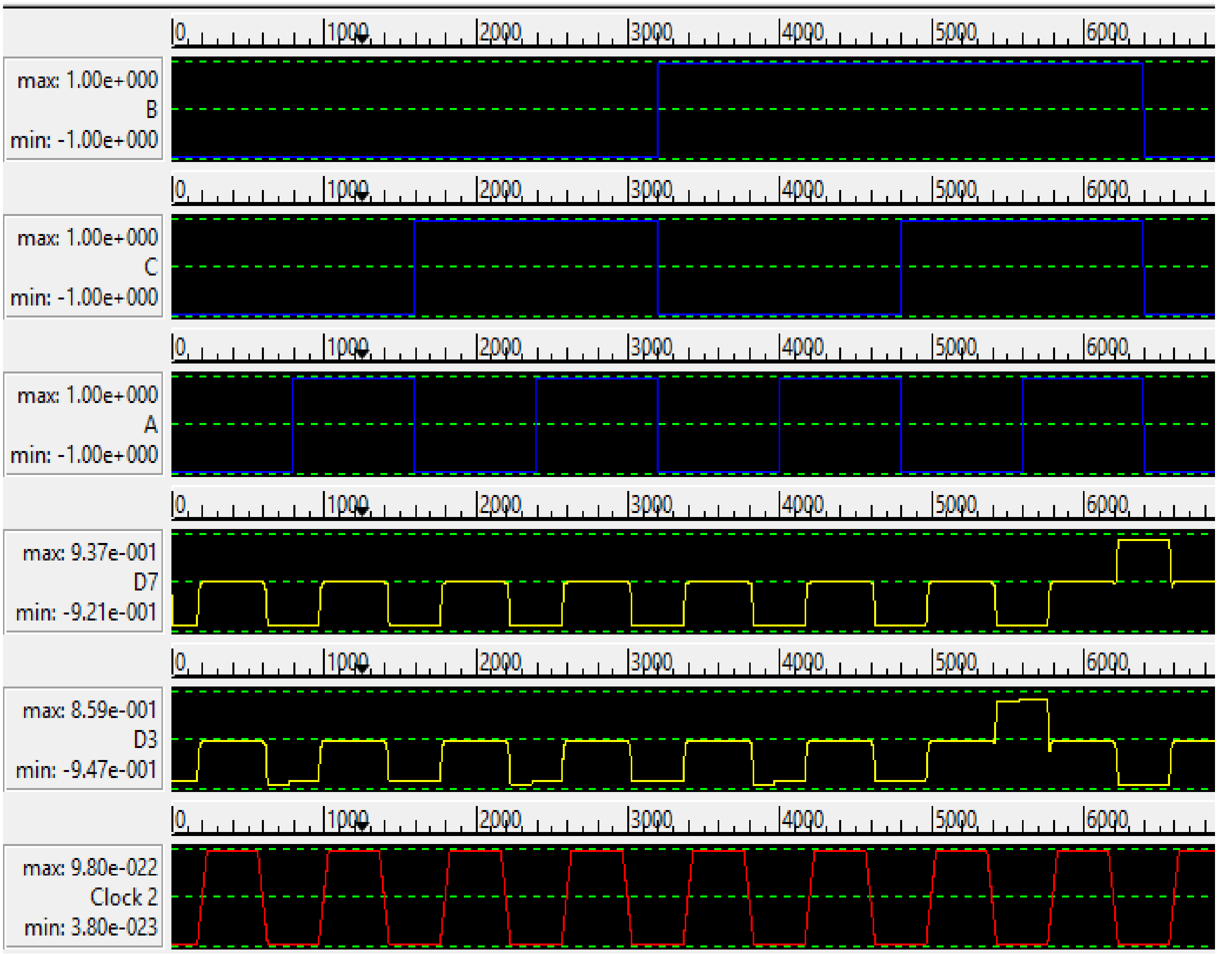



***Figure 9:****Output of D3 and D7*

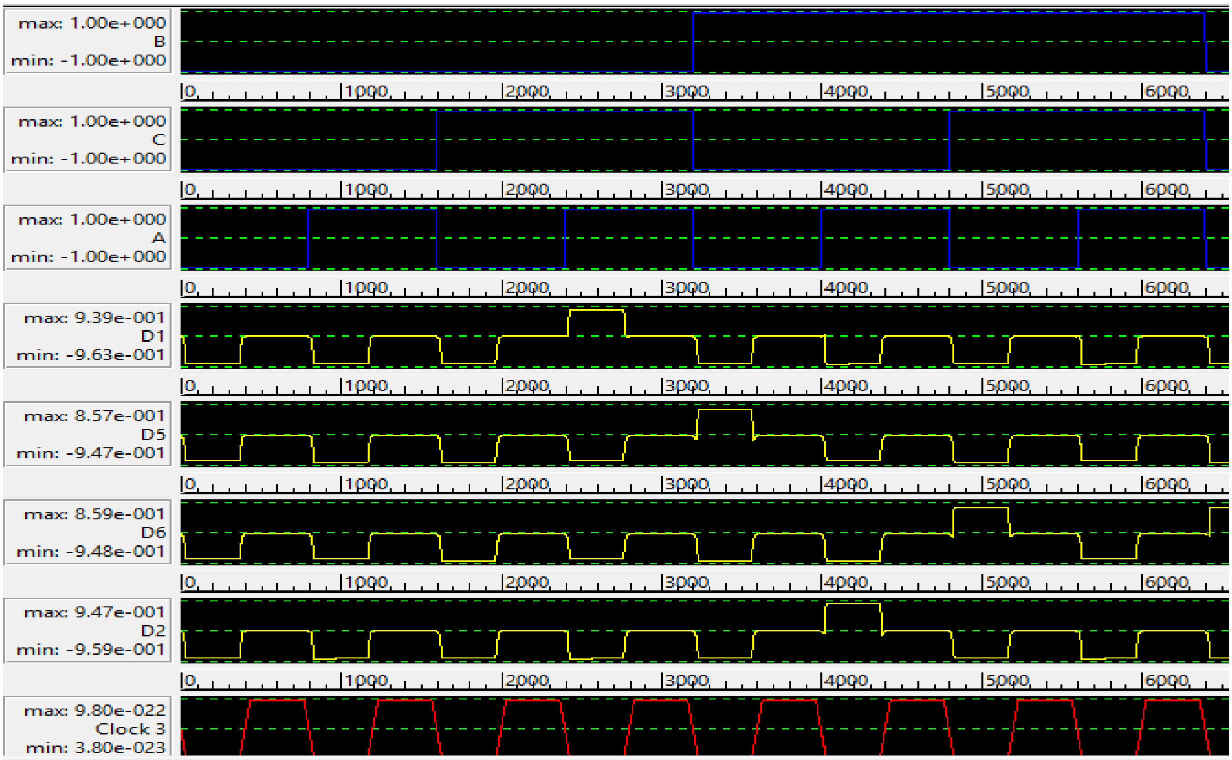



***Figure 10:****Output of D1, D2, D5 and D6.*

***Table 2:** The Results Obtained of the Decoder Circuits in the Existing System.*

| Decoder | Majority gates | Cell count | Area(μm²) |
|---|---|---|---|
| 2X4 | 4 | 60 | 0.06 |
| 3X8 | 12 | 262 | 0.37 |

**PROPOSED SYSTEM**

Our proposed system is 4x2 and 8x3 encoder circuits which is described in Table 3,4 and 5. The proposed system uses the majority gate and simple inverter for the implementation. The number of cells in a QCA circuit is generally proportional to its area. So, by this QCA technology the size of the circuit can be reduced. Figure 11 & 12 explain the QCA design and simulation result of 4×2 encoder. Figure 13 & 14 explain the QCA design and simulation result of 8×3 encoder. Figure 15 & 16 gives the output of X,Y and Z.

***Table 3:** Truth Table of 4X2 Encoder.*

| INPUT | | | | OUTPUT | |
|---|---|---|---|---|---|
| y0 | y1 | y2 | y3 | a | b |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 |

The Boolean expression for 4x2 encoder:

a= y2+y3 andb=y1+y3

**4X2 ENCODER**

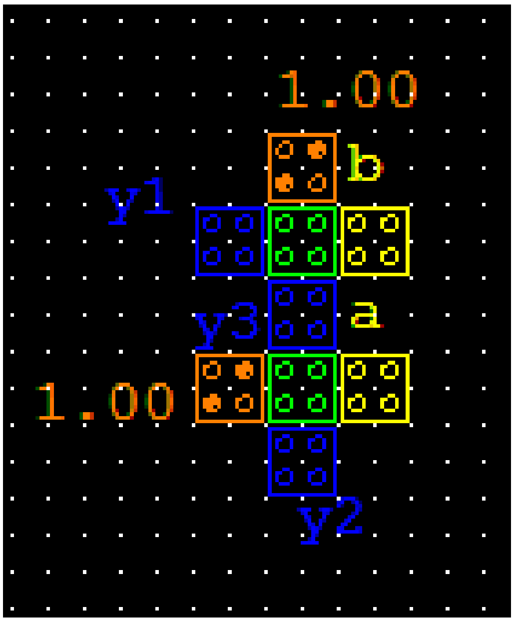



***Figure 11:** QCA Design of 4X2 Encoder.*

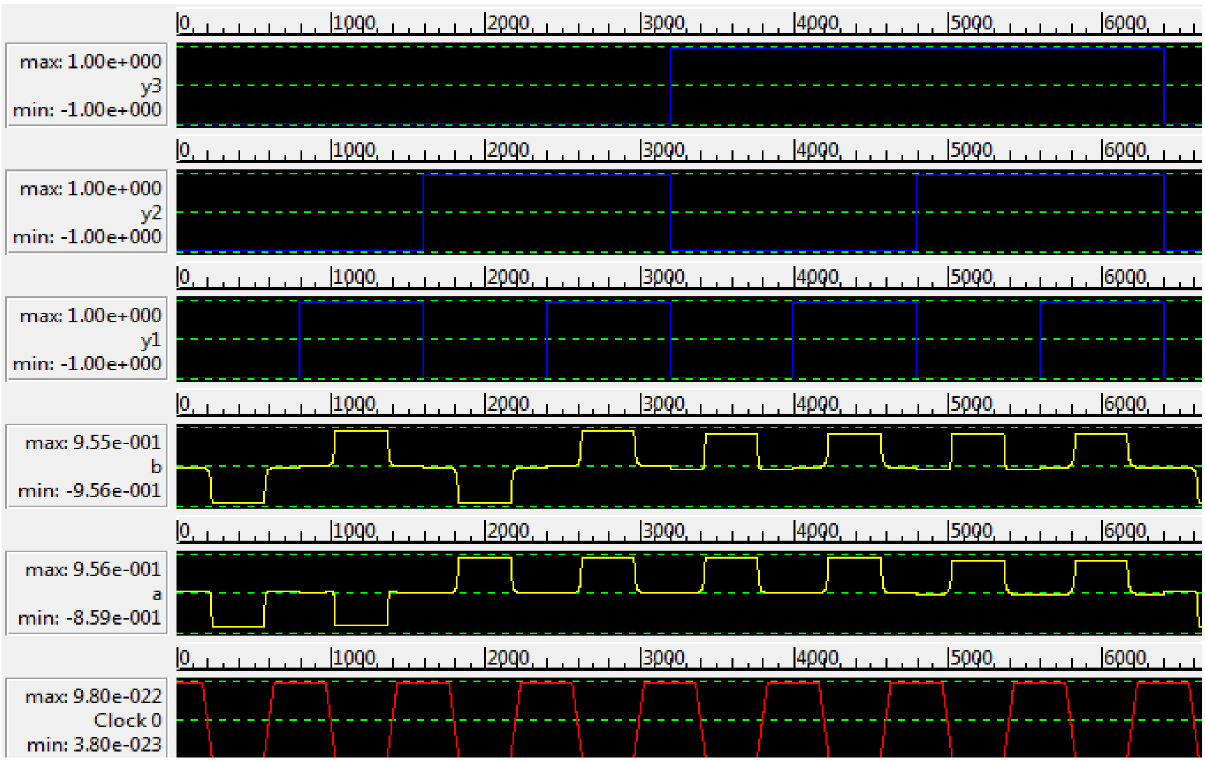



**Figure 12:** *Simulation Result of 4x2 Encoder.*

## 8X3 ENCODER

***Table 4:****Truth Table of 8X3 Encoder*

| INPUT | | | | | | | | OUTPUT | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **D0** | **D1** | **D2** | **D3** | **D4** | **D5** | **D6** | **D7** | **X** | **Y** | **Z** |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

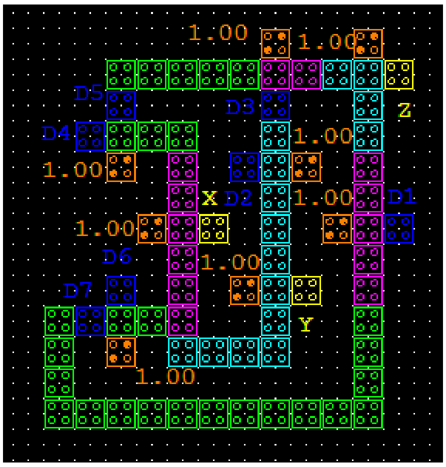



***Figure 13:****QCA Design Of 8x3 Encoder*.

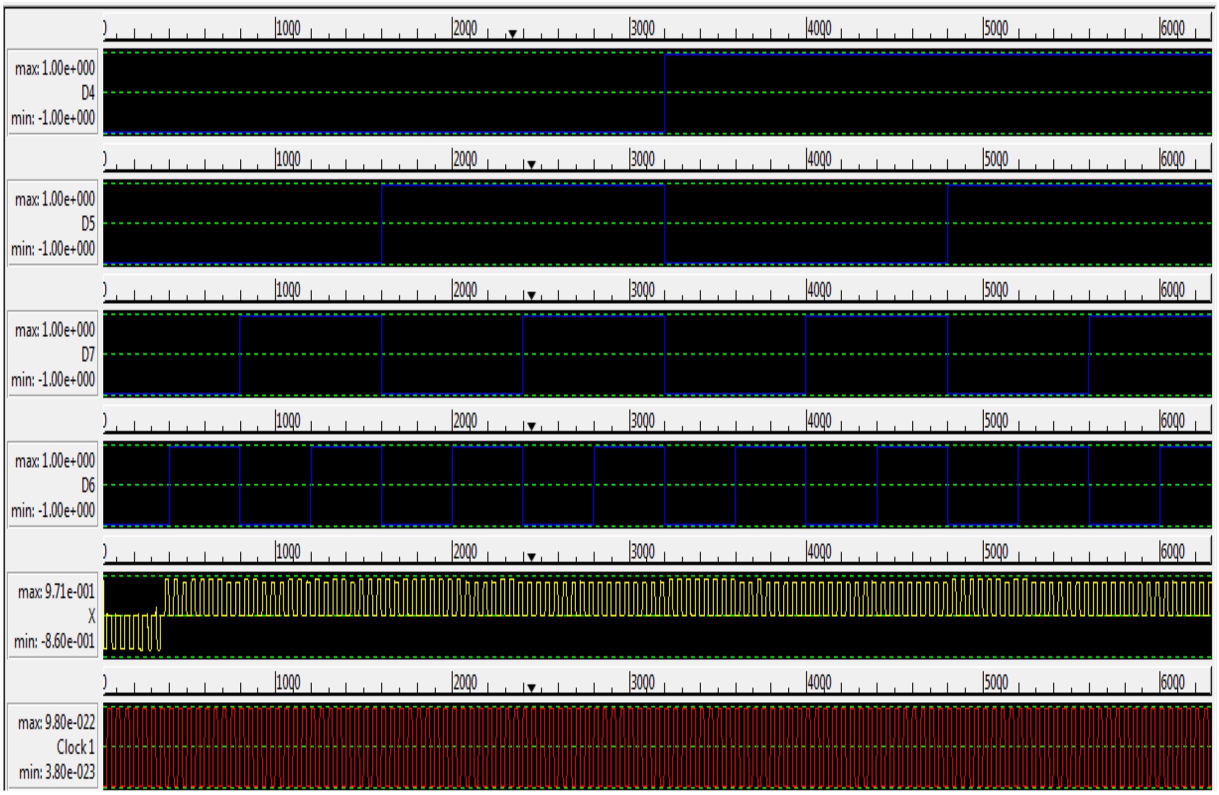



***Figure 14:****Simulation Results OF 8X3 Encoder.*

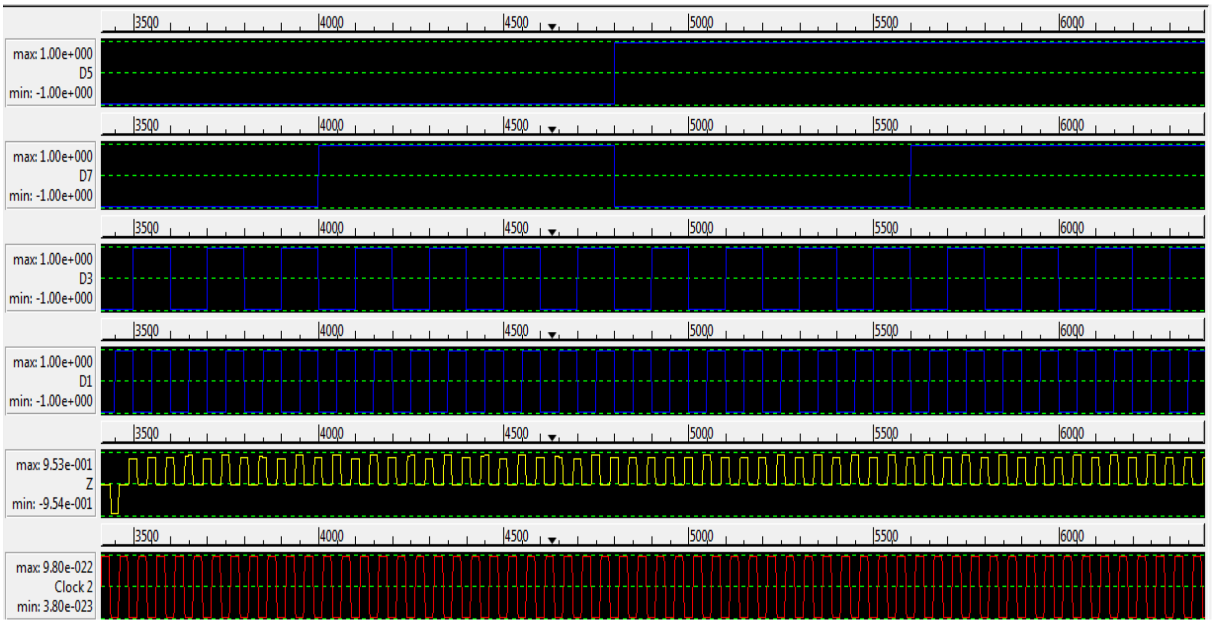



***Figure 15:****Output of Z.*

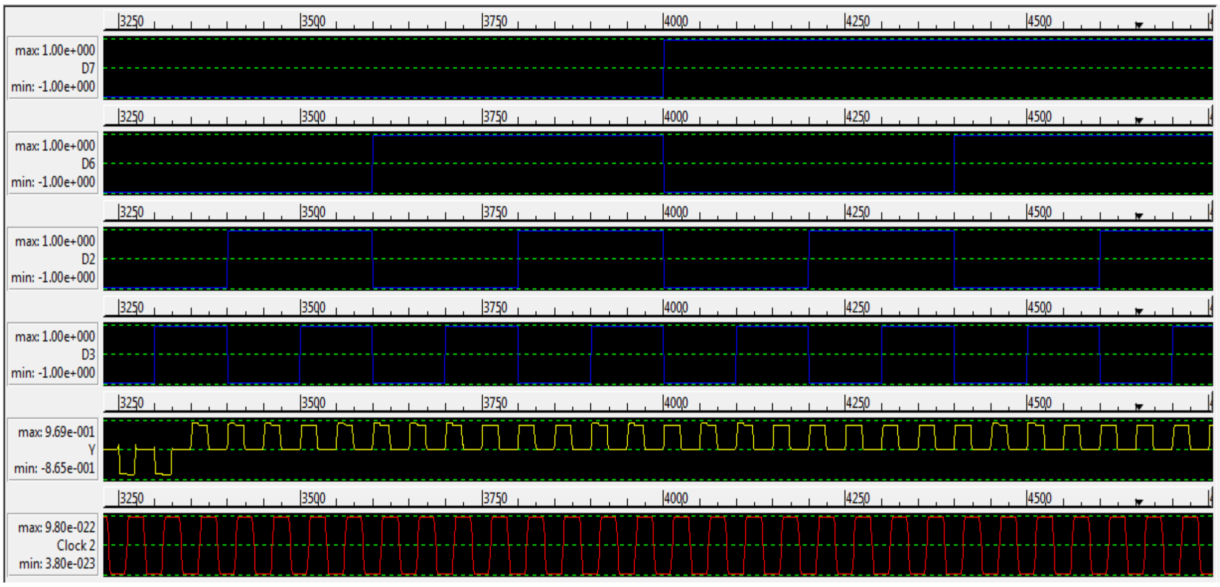



***Figure 16:****Output of Y and  Output of X*

**Table 5:** *The Results Obtained from this Encoder Designs.*

| **Encoder** | **Majority gates** | **Cell count** | **Area( $\mu m^2$)** |
|---|---|---|---|
| 4X2 | 2 | 9 | 0.02 |
| 8X3 | 8 | 73 | 0.07 |

## CONCLUSION

In this paper an optimized and efficient design of 4x2 and 8x3 encoders are implemented and simulated by using QCAD Designer software. Simulation has good performance such as less area, delay and complexity.  An efficient output is obtained in this proposed encoder design by the use of Majority gate and Inverters. The area of the circuit is reduced and the speed of operation is also improved in this design.

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**Cite as:**
A.Chandrasekaran, K. Senthil Kumar, & K.Hemalatha. (2019). Design and Evaluation of a Majority Gate Based Encoder in Quantum-dot Cellular Automata (QCA). Journal of Electronics and Communication Systems, 4(1), 1–11. http://doi.org/10.5281/zenodo.2533577

 